

12/21 Add PJP1 for DCIN Cable on 45 Level
 One for 14W DCIN , PN: DC301001Y00
 Another for 15W DCIN , PN: DC301001V00

05/20 Add DAZ PCB Panel P/N

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JHXXX Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

Laptop Schematics
 (With nVIDIA MXM/B)

2008-06-03

REV: 1.0

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File Name : LA-4241P

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667/800MHz

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	ID1	ID0
JHT00 (00@)	R361	R357
JHT01 (01@)	R361	R355
JHL90 (10@)	R360	R357
JHL91 (11@)	R360	R355

MIC ID Table

R	Structure
R585 Single MIC	SINGLE@
R583 Array MIC	DUAL@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM (24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

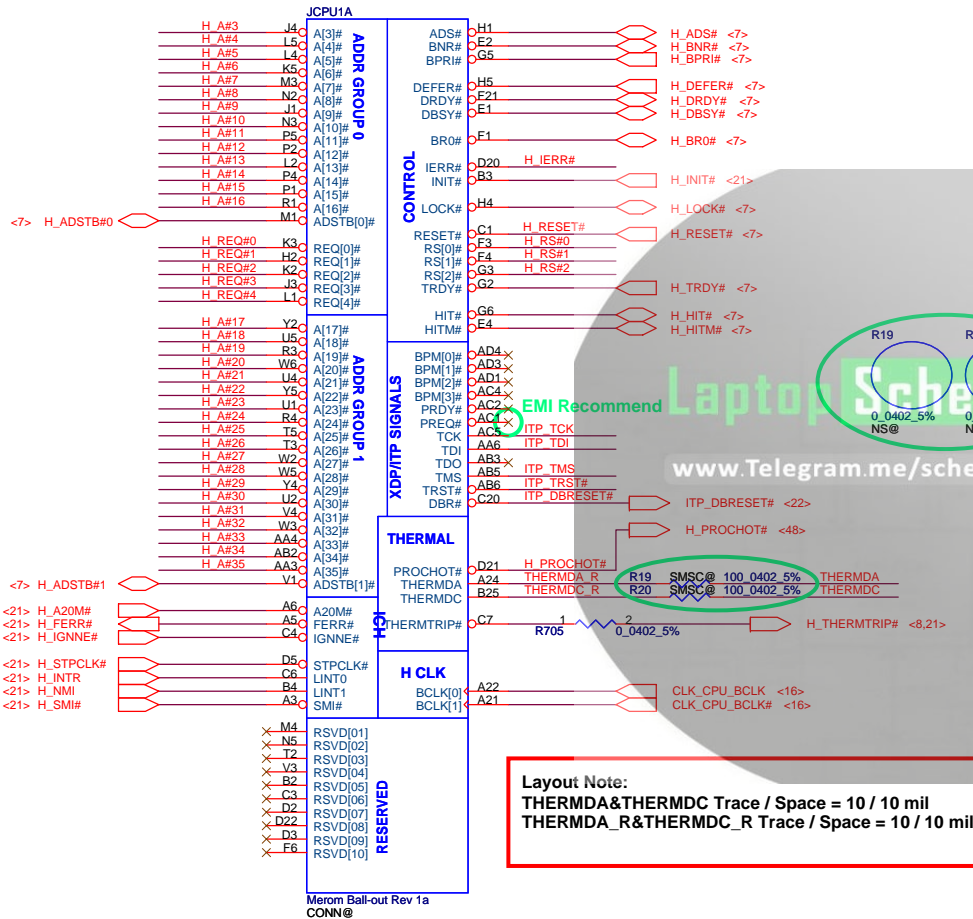
SKU ID Table

Vcc	3.3V +/- 5%
Rb	47K +/- 5%

Rb~ R470
Ra~ R472

Board ID	Rb	Ra	VAD_BID min	VAD_BID typ	VAD_BID max	Ra BOM Structure
1	NA	4.7K +/- 5%	0 V	0 V	0 V	H_14_B@
2	47K (RB@)	4.7K +/- 5%	0.274 V	0.300 V	0.328 V	H_14_C@ ✓
3	47K (RB@)	10K +/- 5%	0.553V	0.578 V	0.628 V	H_14_MP@
4	47K (RB@)	18K +/- 5%	0.849V	0.913V	0.981 V	H_15_B@
5	47K (RB@)	27K +/- 5%	1.129 V	1.204 V	1.282 V	H_15_C@ ✓
6	47K (RB@)	39K +/- 5%	1.415 V	1.496 V	1.579 V	H_15_MP@
7	47K (RB@)	56K +/- 5%	1.712 V	1.794 V	1.876 V	L_14_B@
8	47K (RB@)	82K +/- 5%	2.020V	2.097 V	2.173 V	L_14_C@ ✓
9	47K (RB@)	120K +/- 5%	2.303 V	2.371 V	2.437 V	L_14_MP@
10	47K (RB@)	220K +/- 5%	2.670 V	2.719 V	2.765 V	L_15_B@
11	47K (RB@)	470K +/- 5%	2.972 V	3.000 V	3.026 V	L_15_C@ ✓
12	47K (RB@)	NA	3.135 V	3.300 V	3.465 V	NA for L_15_MP

<7> H_A# [3..35]
 <7> H_REQ# [0..4]
 <7> H_RS# [0..2]



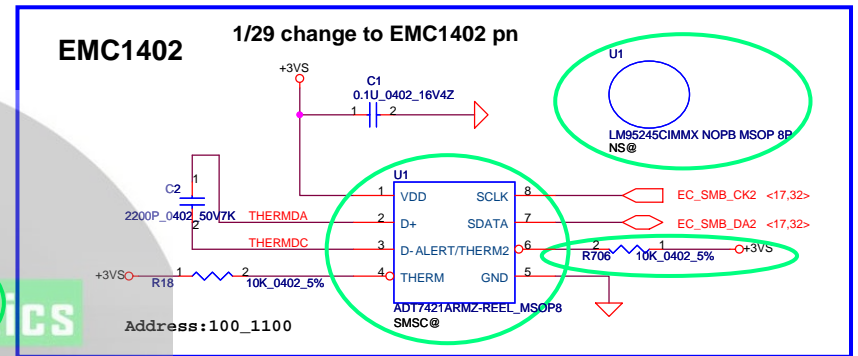
Layout Note:
 THERMDA&THERMDC Trace / Space = 10 / 10 mil
 THERMDA_R&THERMDC_R Trace / Space = 10 / 10 mil

Which to follow?

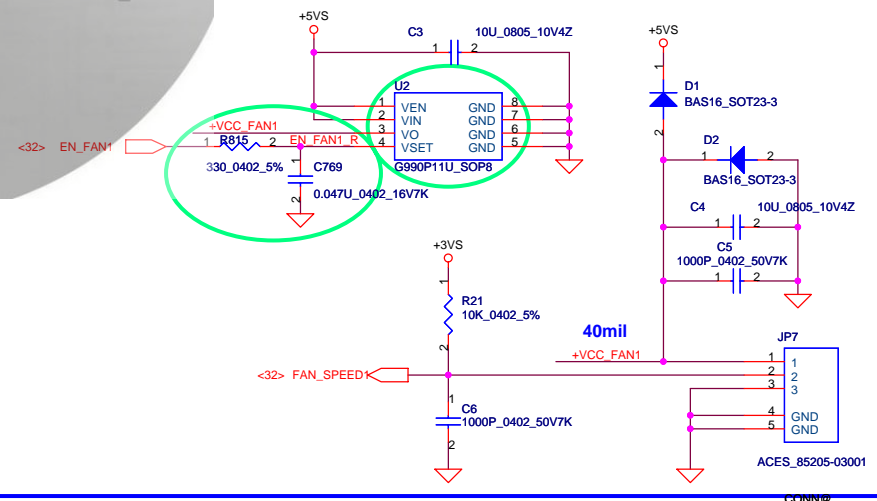
	Checklist	CRB
TCK	55_5%	54.9_1%
TDI	55_5%	54.9_1%
TMS	55_1%	54.9_1%
TRST#	55_5%	54.9_1%
PREQ#	x	54.9_1%

EMI Recommend

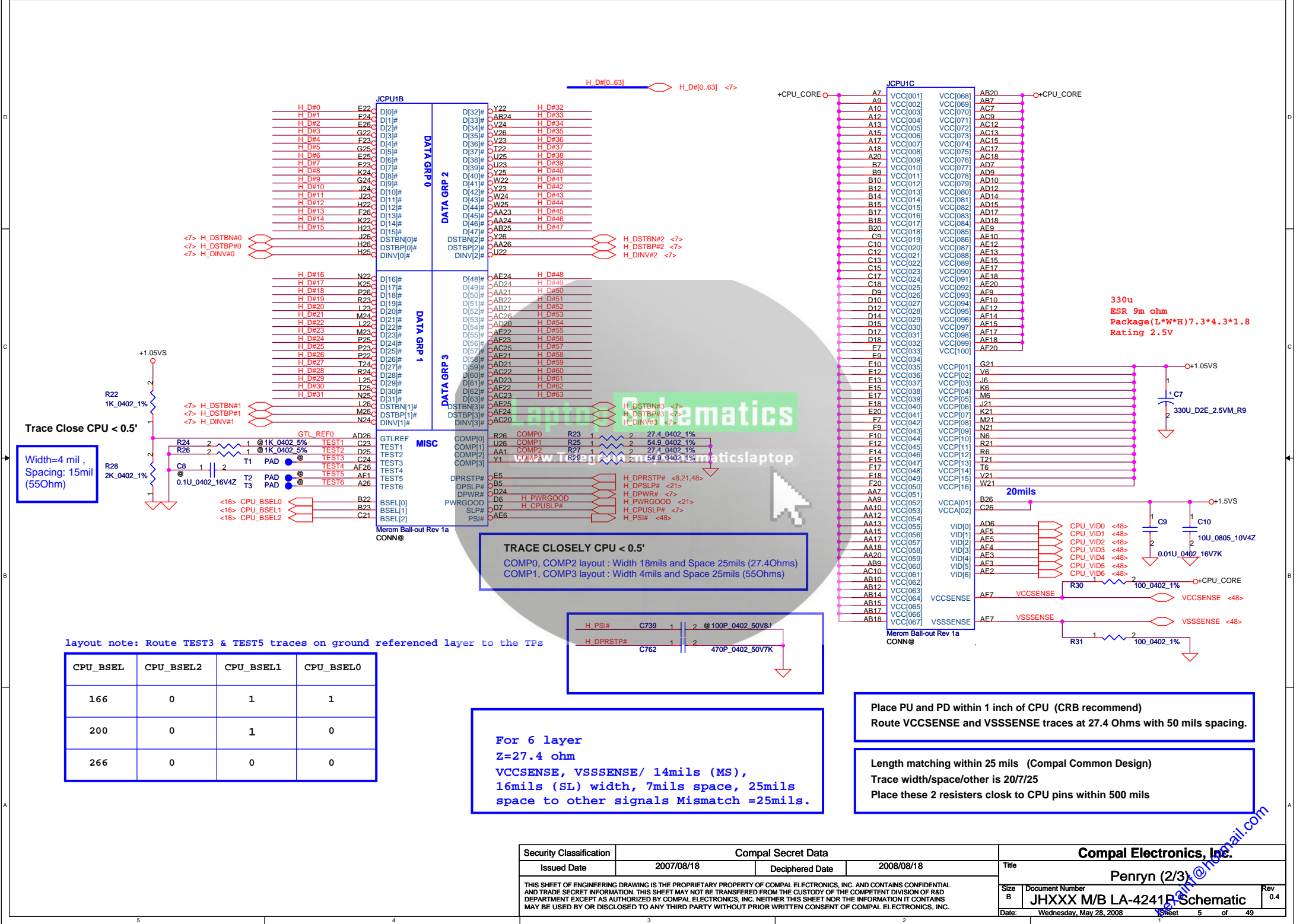
H_IERR#	R12	1	2	56_0402_5%
ITP_TMS	R13	1	2	54.9_0402_1%
ITP_TDI	R14	1	2	54.9_0402_1%
H_PROCHOT#	R15	1	2	56_0402_5%
ITP_TCK	R16	1	2	54.9_0402_1%
ITP_TRST#	R17	1	2	54.9_0402_1%



FAN1 Conn



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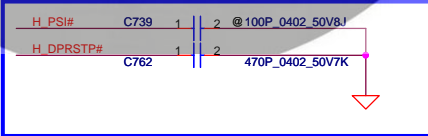
Trace Close CPU < 0.5'

Width=4 mil ,
Spacing: 15mil
(550hm)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs			
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

TRACE CLOSELY CPU < 0.5'

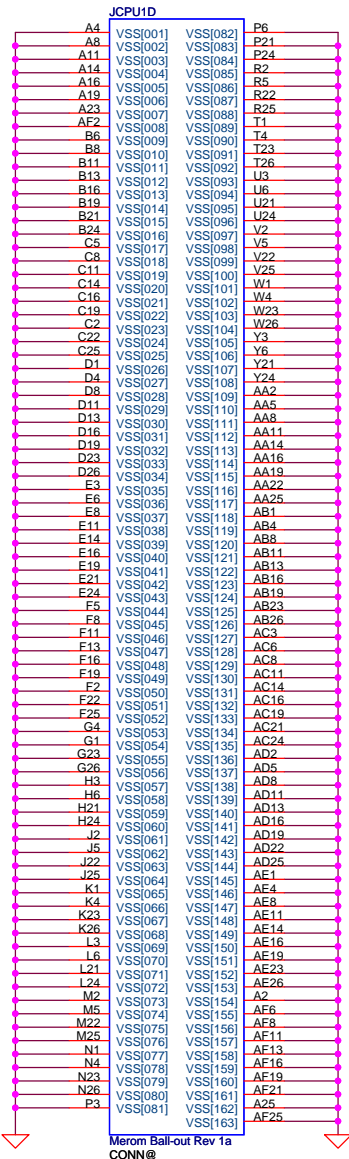
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (550hm)



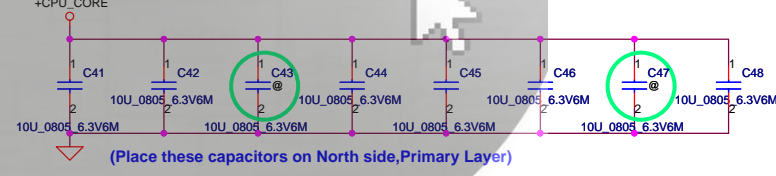
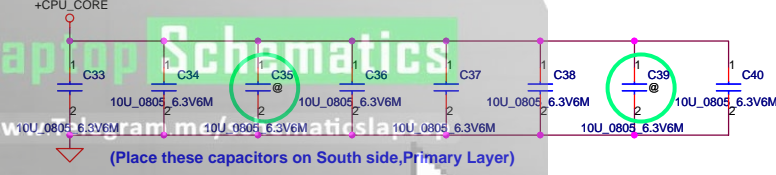
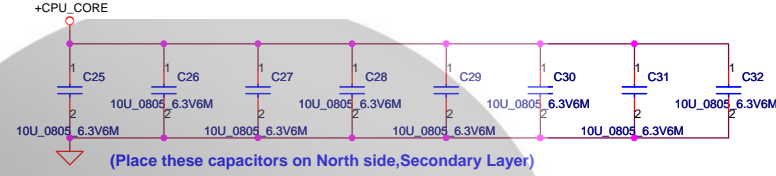
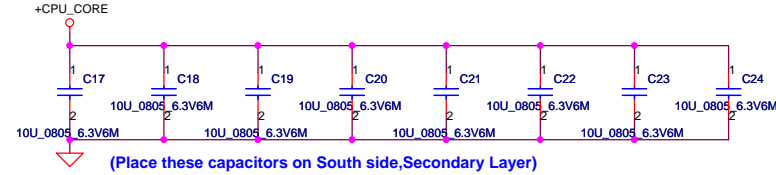
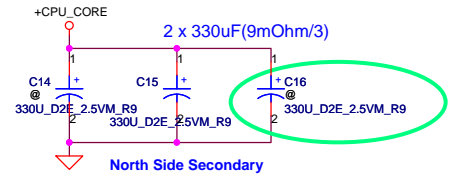
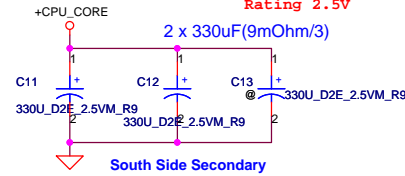
For 6 layer
Z=27.4 ohm
VCCSENSE, VSSSENSE/ 14mils (MS),
16mils (SL) width, 7mils space, 25mils
space to other signals Mismatch =25mils.

Place PU and PD within 1 inch of CPU (CRB recommend)
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mils spacing.

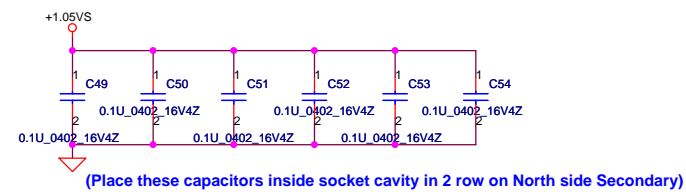
Length matching within 25 mils (Compal Common Design)
Trace width/space/other is 207/25
Place these 2 resistors close to CPU pins within 500 mils



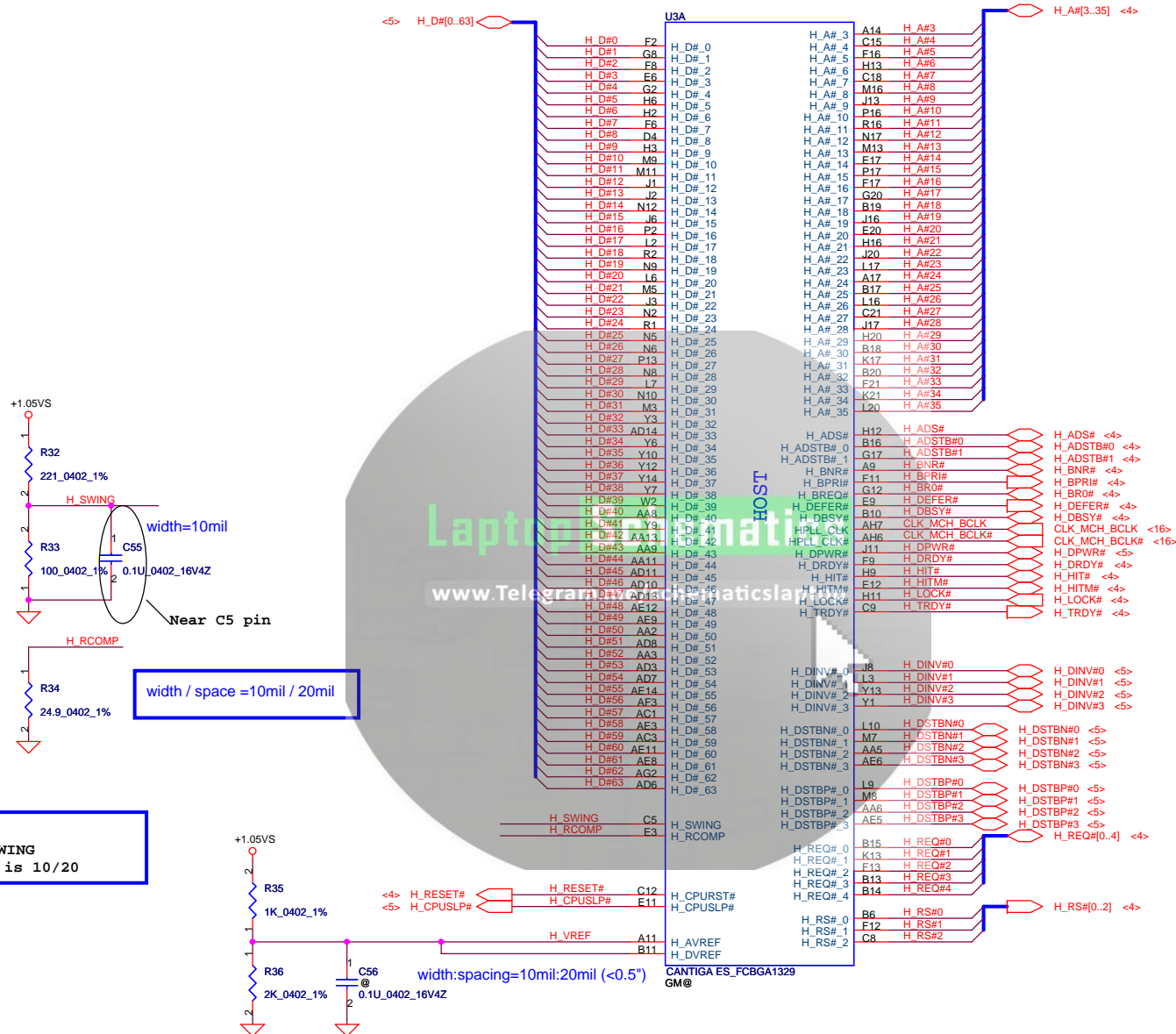
330u
ESR 9m ohm
Package (L*W*H) 7.3*4.3*1.8
Rating 2.5V



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

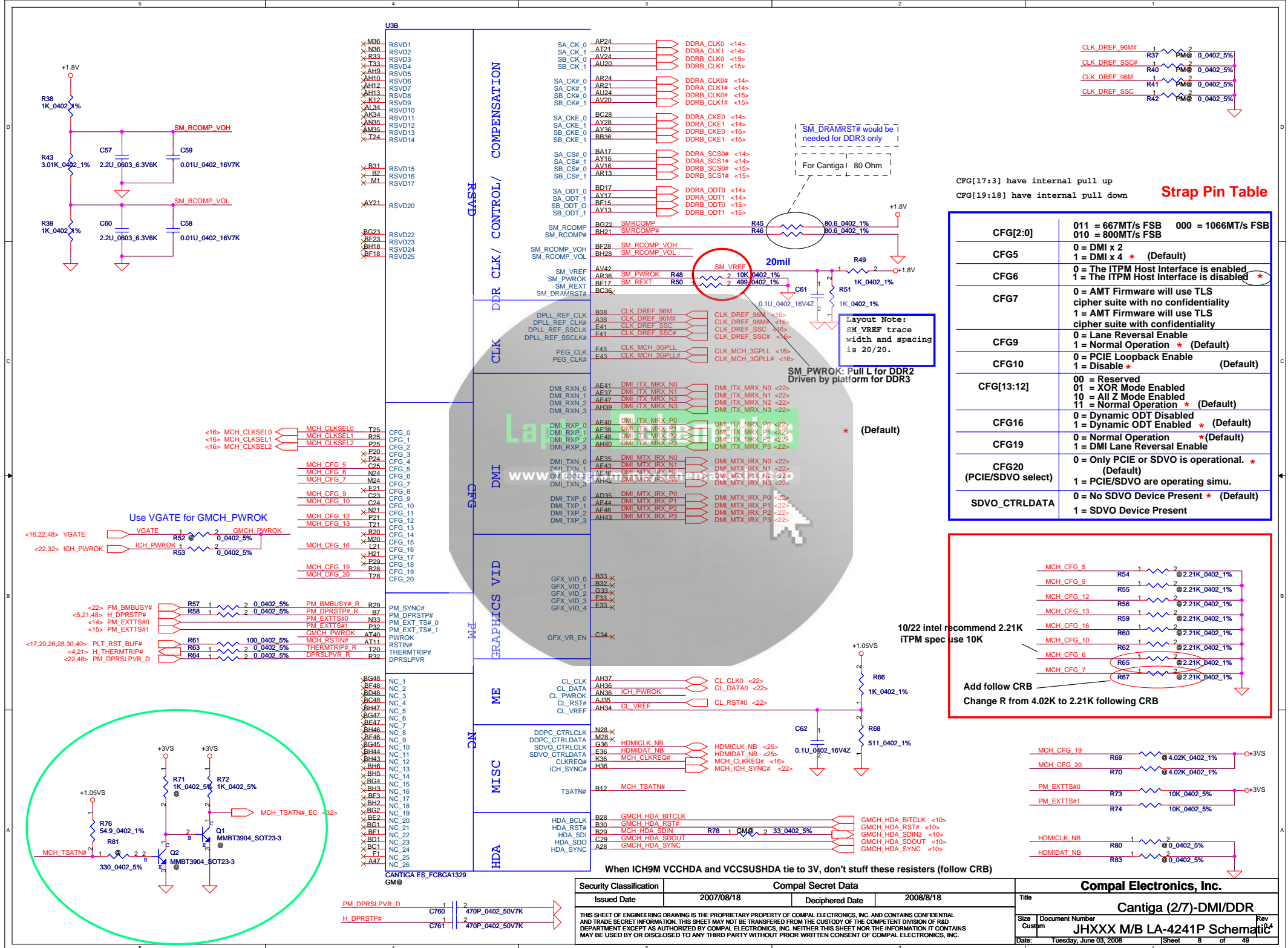


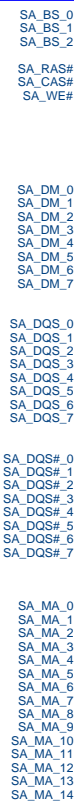
Change U3 from SA00001P900 to SA00001P930
3/4 Change U3 from SA00001P930 to SA00002JT10 (B0 to B2)



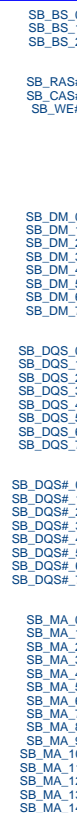
Layout Note:
H_RCOMP / H_VREF / H_SWING
trace width and spacing is 10/20

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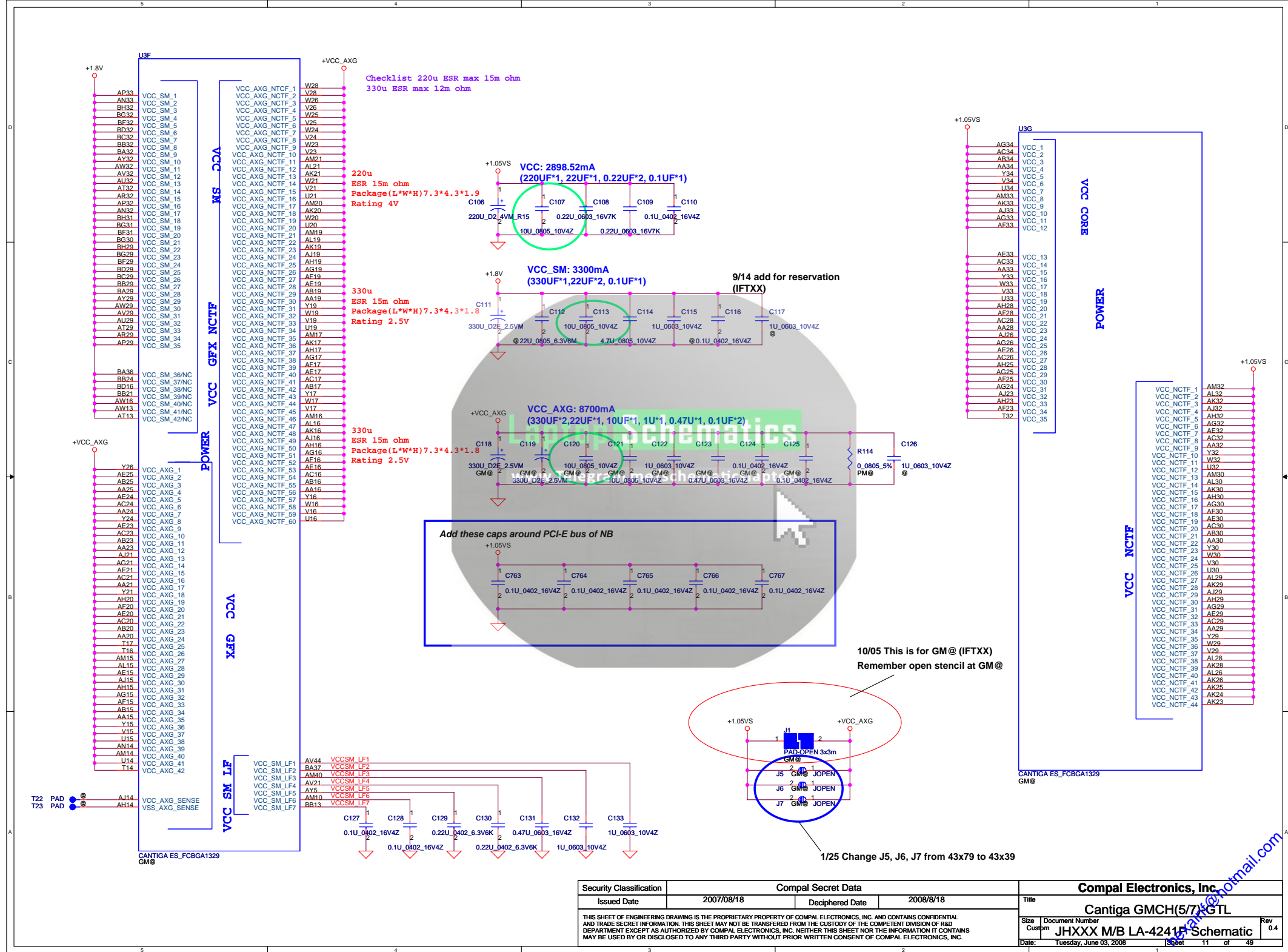


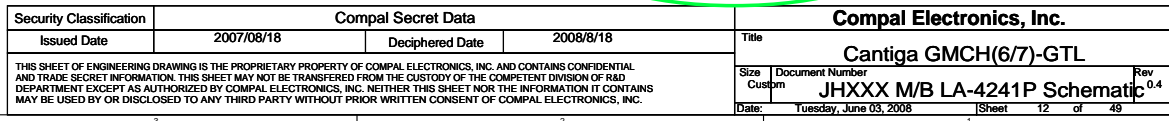
CANTIGA ES FCBGA1329

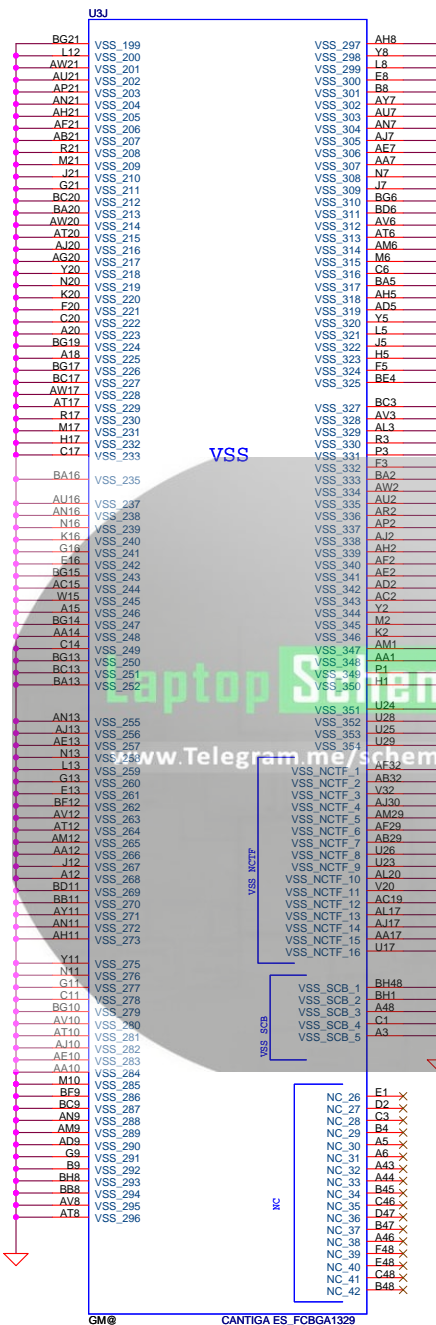
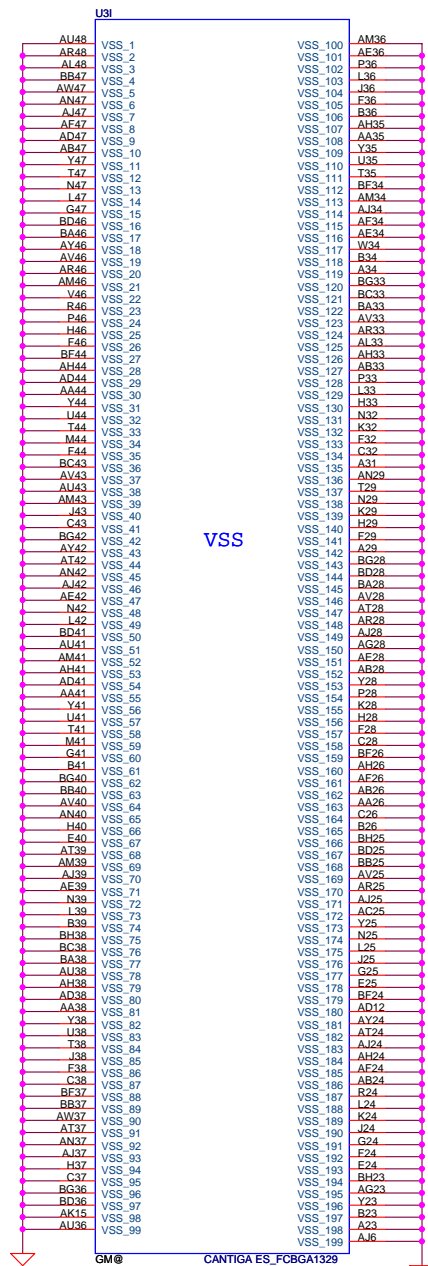


CANTIGA ES FCBGA1329

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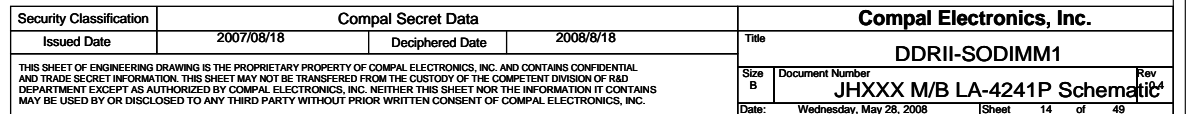




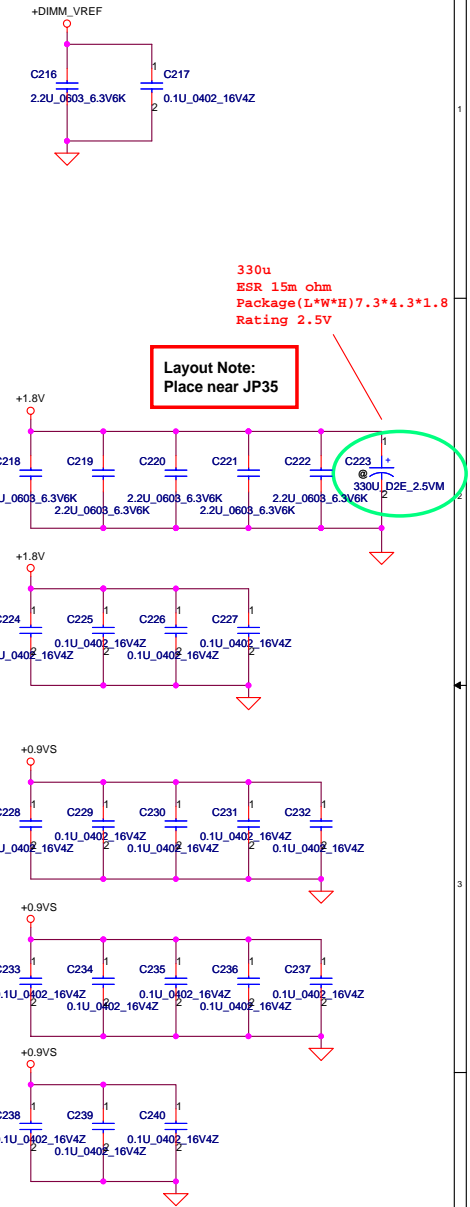


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DIMM1 STD H:5.2mm (BOT)



DIMM2 STD H:9.2mm (BOT)







Layout Note:
Place near JP35

330u
ESR 15m ohm
Package(L*W*H)7.3*4.3*1.8
Rating 2.5V

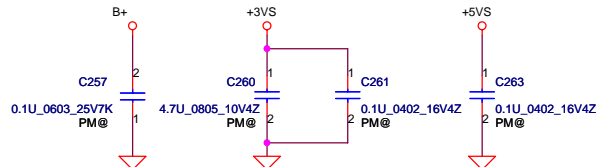
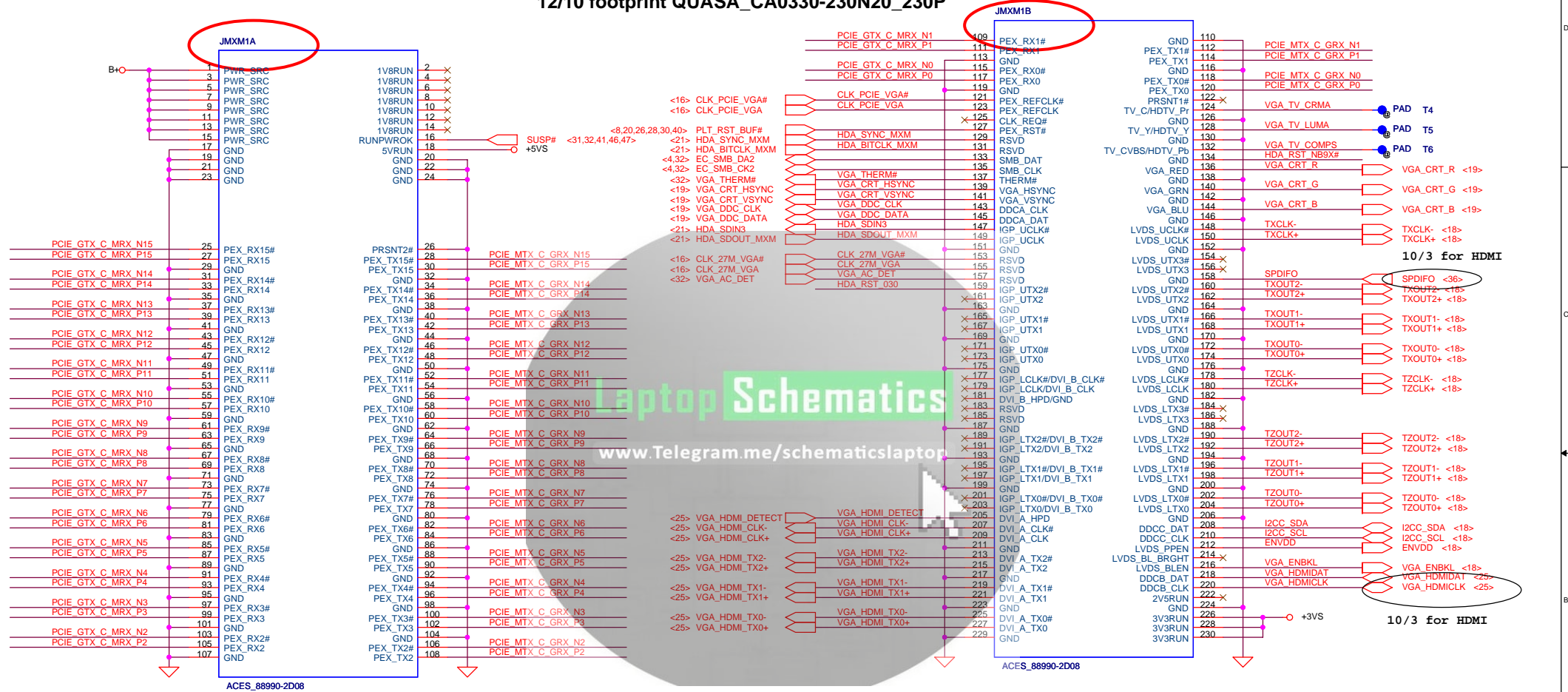
Layout Note:
Place these resistor
closely JP35,all
trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

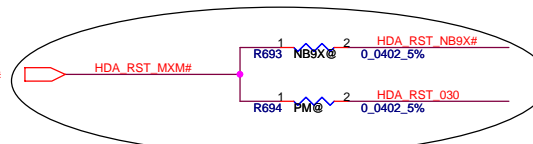
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<10,25> PCIE_MTX_C_GRX_N[0..15]  PCIE_MTX_C_GRX_N[0..15]
<10,25> PCIE_MTX_C_GRX_P[0..15]  PCIE_MTX_C_GRX_P[0..15]
<10> PCIE_GTX_C_MRX_N[0..15]  PCIE_GTX_C_MRX_N[0..15]
<10> PCIE_GTX_C_MRX_P[0..15]  PCIE_GTX_C_MRX_P[0..15]

9/13 modify this footprint from ACES_88990-2D08_230P to ACES_88990-2D28_230P
12/19 modify this footprint from ACES_88990-2D28_230P to QUASA_CA0330-230N20_230P
0208 : Modify this footprint from QUASA_CA0330-230N20_230P to QUASA_CA0330-230N20_230P-S
12/10 footprint QUASA_CA0330-230N20_230P



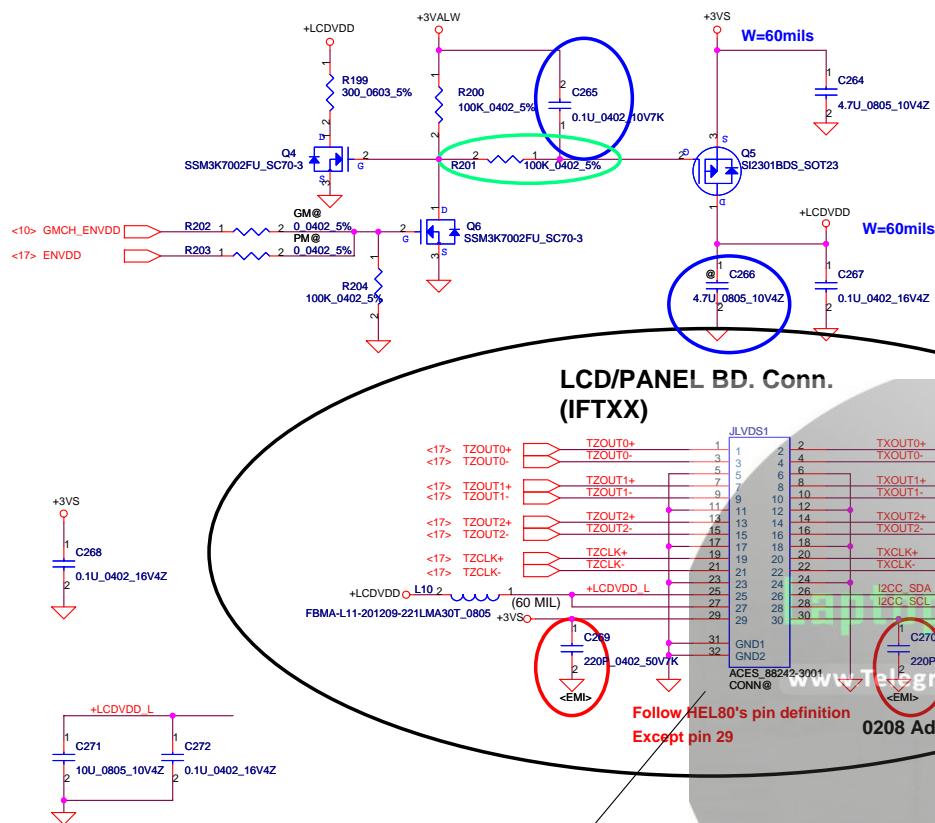
<21> HDA_RST_MXM#



SPDIFO	R198	1	2	0.0402 5%
		R693	R694	
NB9X	Mount	No stuff		
030 NB9X	No stuff	Mount		
NB8X	No stuff	No stuff		

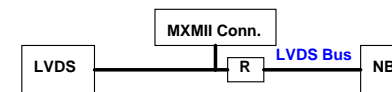
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LCD POWER CIRCUIT

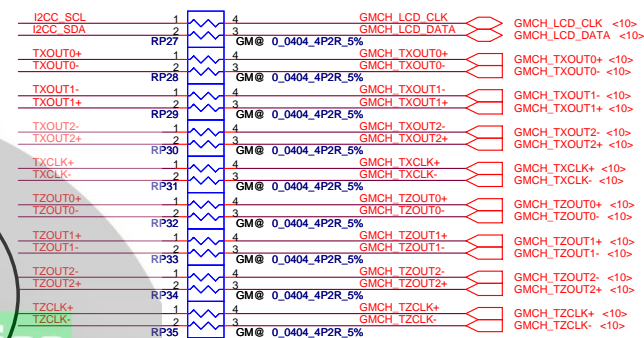


LTCX000G500 footprint is still use ACES_88242-3001

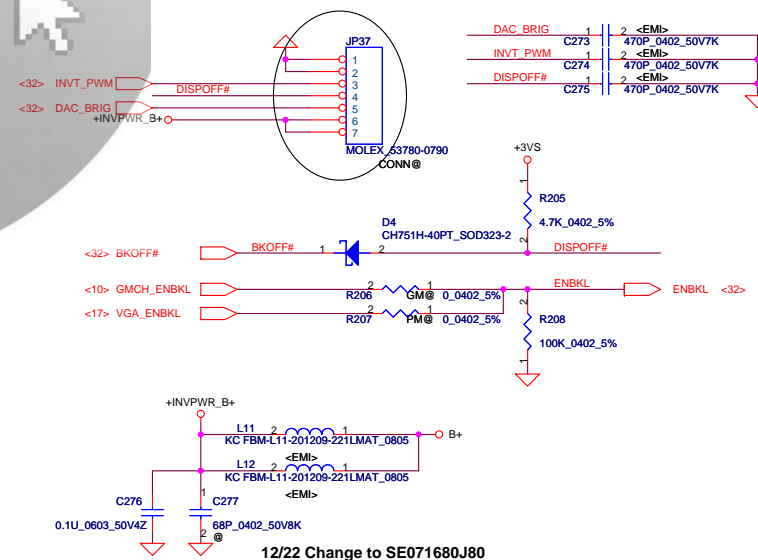
Routing Diagram



Use Daisy chain to route

**INVERTER Conn.**

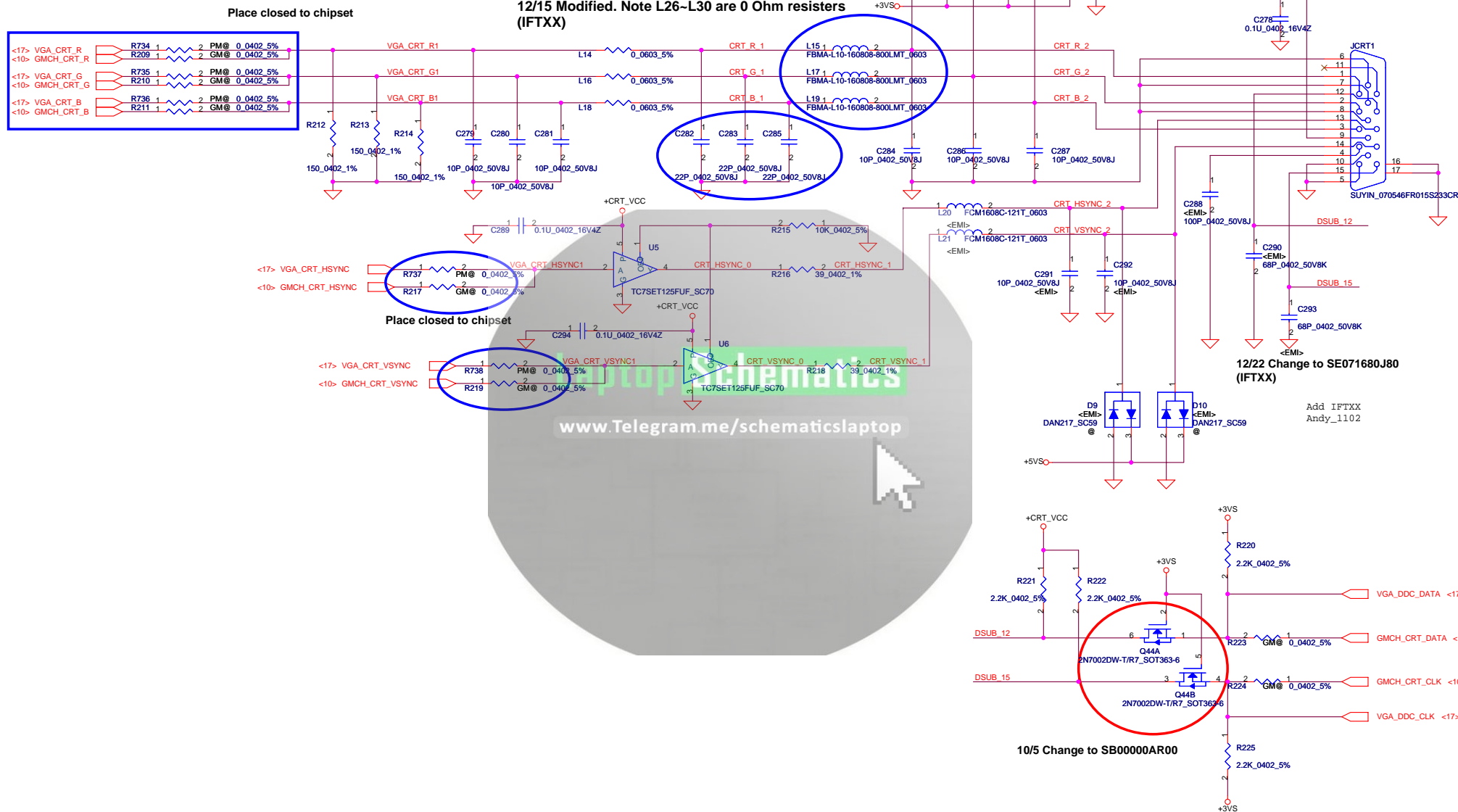
12/18 modified from
220p @ to 470p mount
by EMI request



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				LVDS & DVI Connector	
				Size B	Document Number
				JHXXXX M/B LA-4241P Schematic	
				Date:	Wednesday, May 28, 2008
				Sheet	18 of 49

CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p



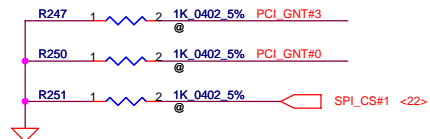
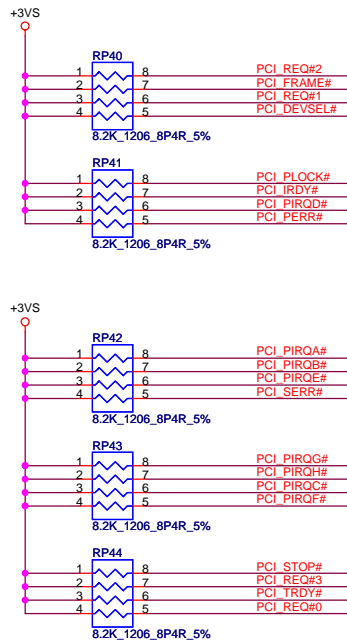
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Size	Document Number
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				Sheet	19 of 49

Compal Electronics, Inc.

CRT Connector

JHXXX M/B LA-4241P Schematic

Rev

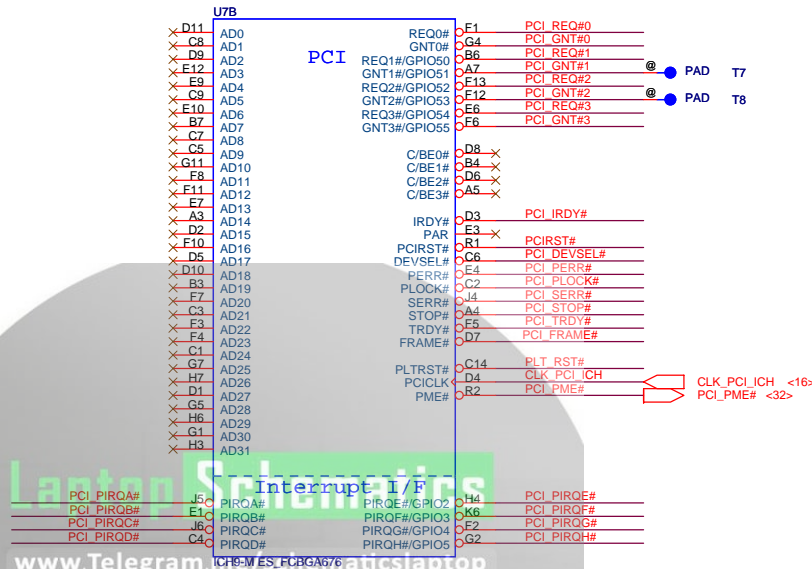


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

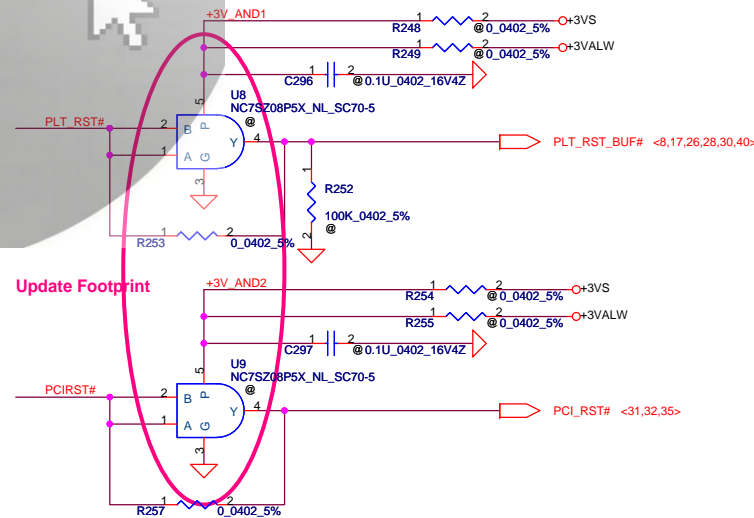
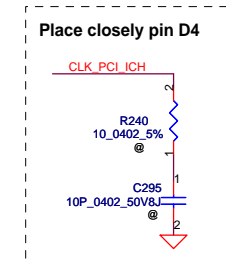
CRB: GNT#0 and SPI_CS#1 have a weak internal pull up

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

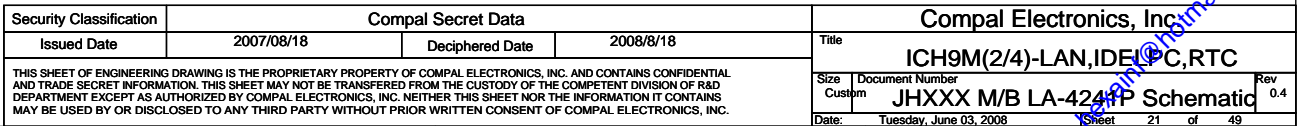
3/4 Change U7 from SA00002AN10 to SA00002JH00 (A2 to A3)

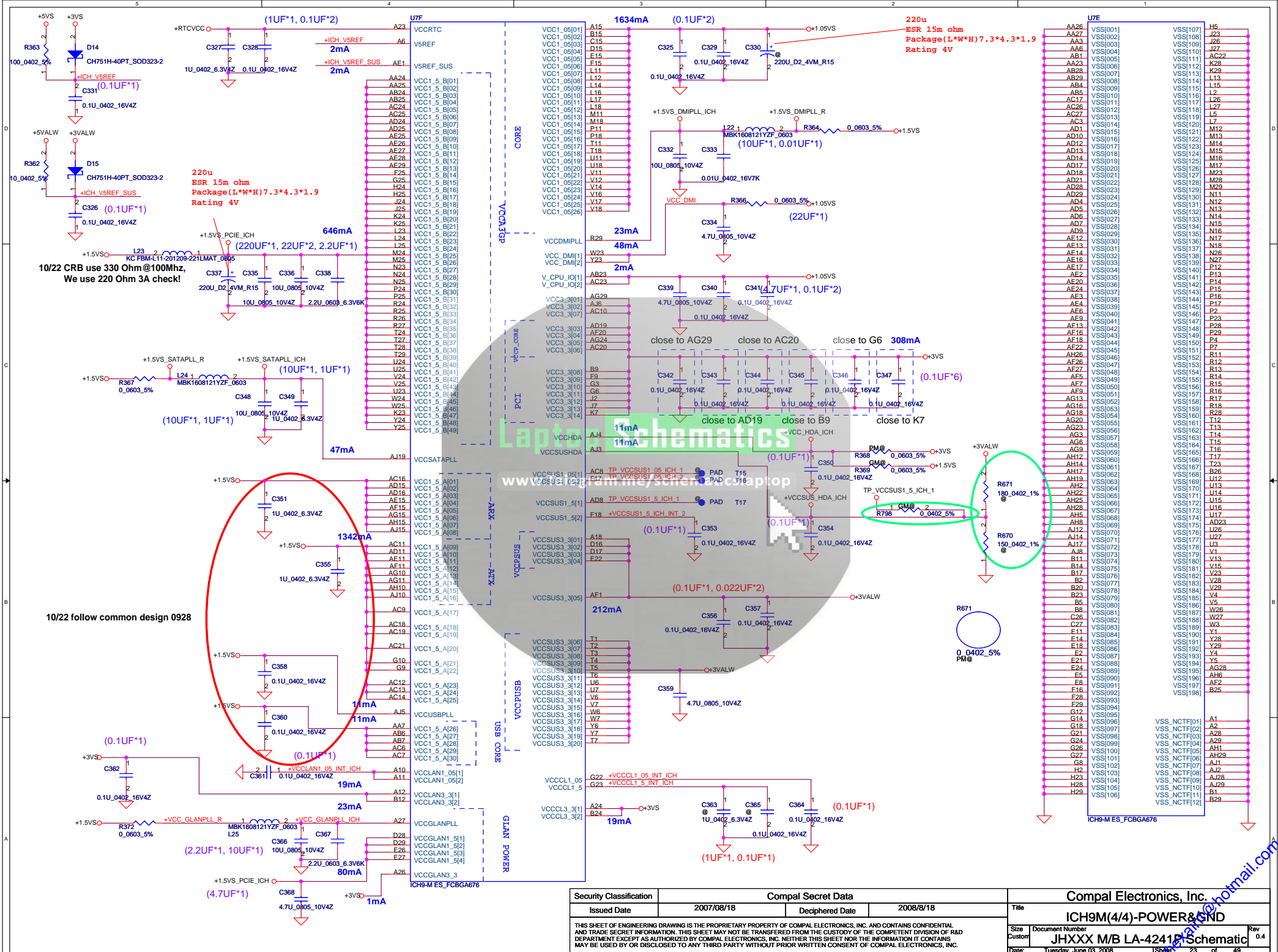


DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



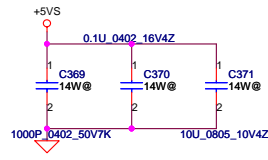
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	
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Size		Document Number		Rev	
Date		Tuesday, June 03, 2008		Sheet 20 of 49	





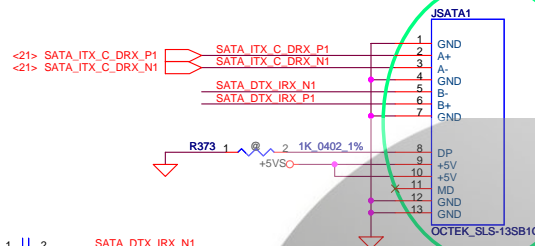
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				ICH9M(4/4)-POWER&GND		
				Size		
Customer		Document Number			Rev	
		JHXXX M/B LA-4241P Schematic			0.4	
Date:		Tuesday, June 03, 2008		Sheet		23 of 49

14W SATA ODD Conn.



SATA ODD Conn.

Copy JIWA2 Symbol

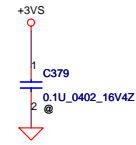
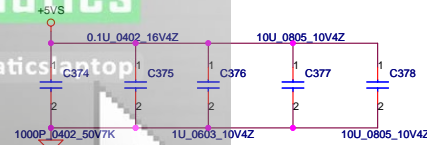


Update FootPrint from
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OCTEK_SLS-13SB1G_13P_RV-T

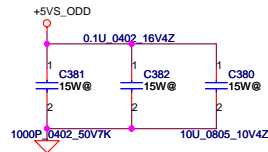
Laptop Schematics

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SATA HDD Conn.

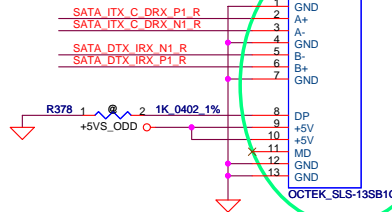
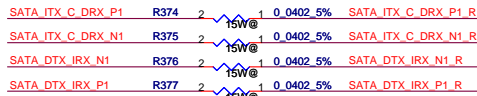


15W SATA ODD Conn.

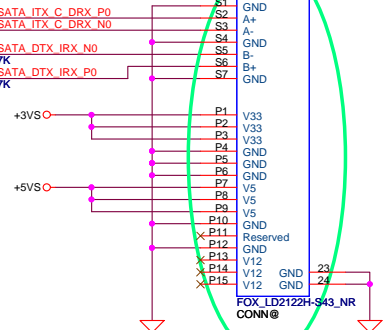
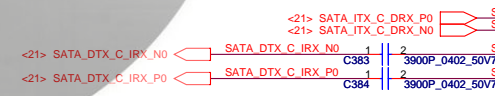


SATA ODD Conn.

Copy JIWA2 Symbol

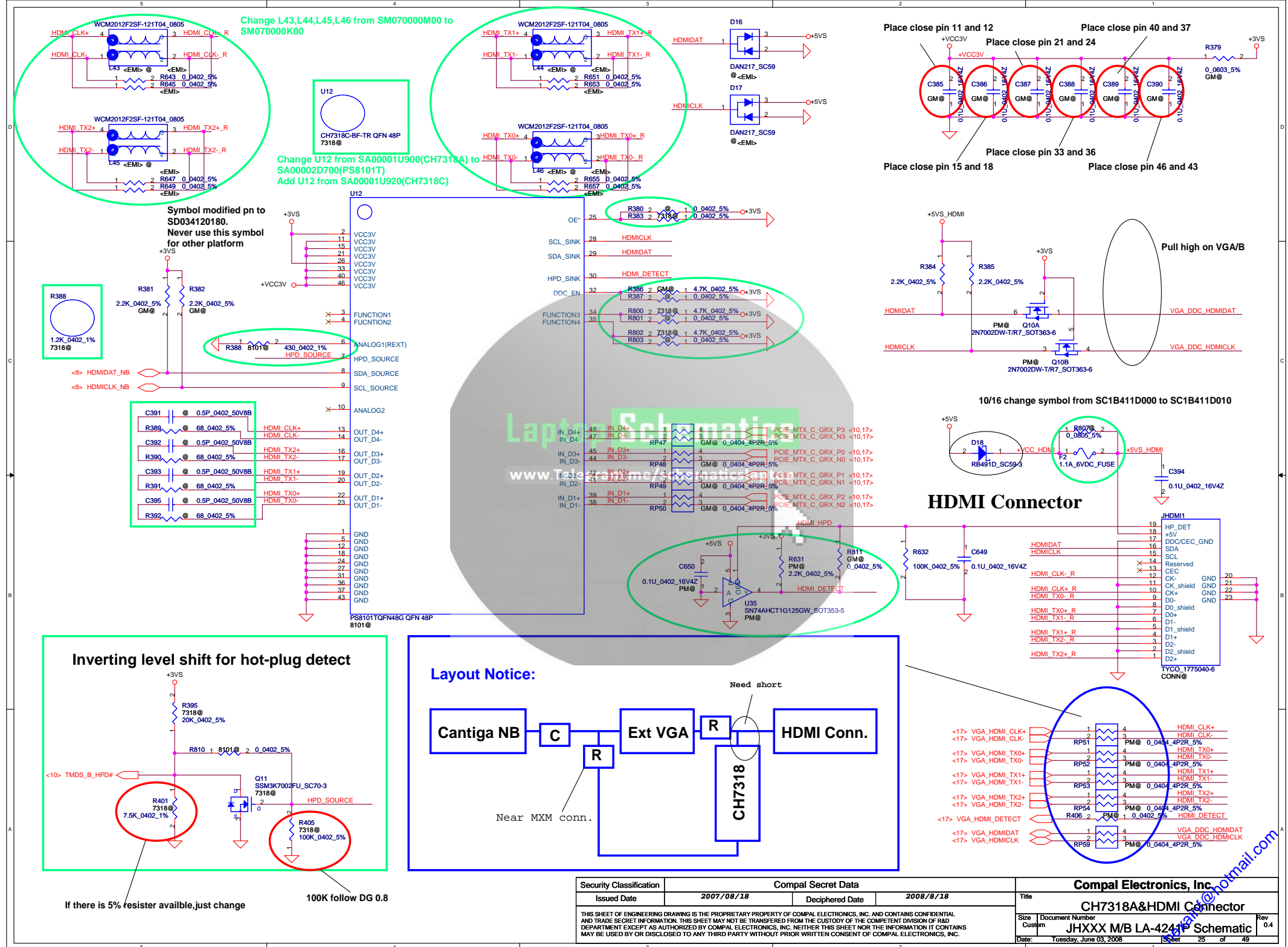


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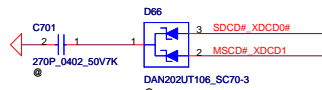
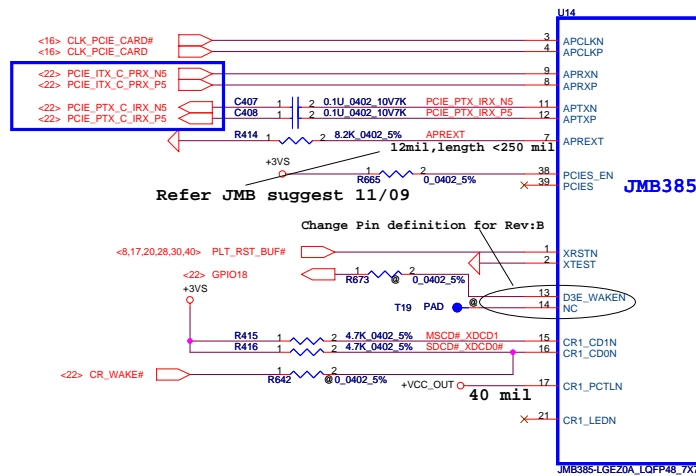
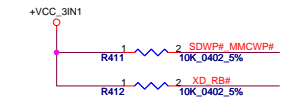
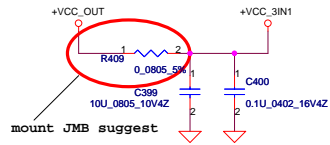


Update Symbol
SP01000G800
FOX_LD2122H-S43_NR
Manually update pin number

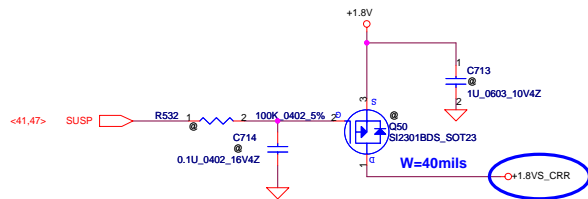
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Title		Compal Electronics, Inc.	
HDD & ODD Connector		JHXXX M/B LA-4241P Schematic	
Size	Document Number	Rev	4
Date:	Wednesday, May 28, 2008	Sheet	24 of 49



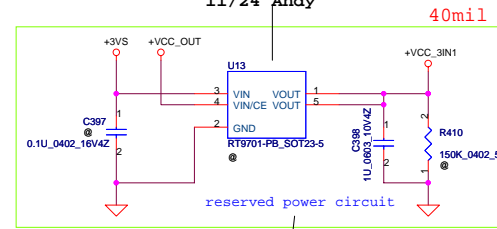
Use 0805 type and over 20 mils trace width on both side



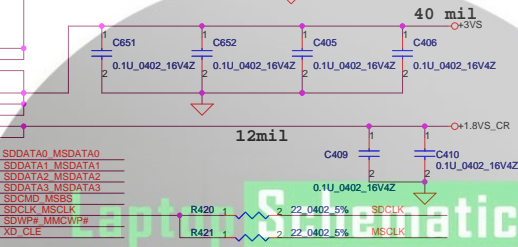
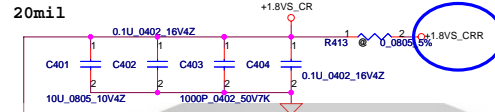
Rev :B



Active High EN
11/24 Andy



Refer JMB suggest 11/14

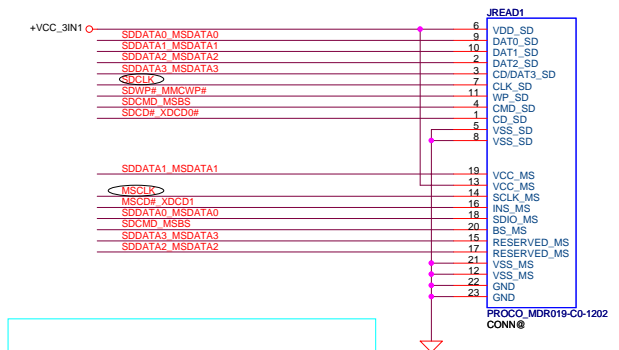


Strap pin for JMicro

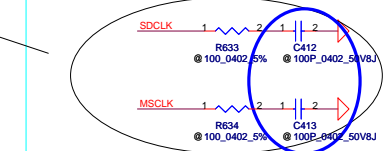
Refer JMB suggest 11/09

SD,MMC,MS multi-function pin define		
MDIO PIN Name	SD/MMC Card PIN Name	MS Card PIN Name
MDIO00	SD1_DAT0	MS1_DAT0
MDIO01	SD1_DAT1	MS1_DAT1
MDIO02	SD1_DAT2	MS1_DAT2
MDIO03	SD1_DAT3	MS1_DAT3
MDIO04	SD1_CMD	MS1_BS
MDIO05	SD1_CLK	MS1_CLK
MDIO06	SD1_WP	
MDIO07		
MDIO08	MMC_DAT4	MS1_DAT4
MDIO09	MMC_DAT5	MS1_DAT5
MDIO10	MMC_DAT6	MS1_DAT6
MDIO11	MMC_DAT7	MS1_DAT7
MDIO12		
MDIO13		
MDIO14		
CR1_LEDN	SD1_LED#	MS1_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#
CR1_CD0	SD1_CD#	
CR1_CD1		MS1_CD#

3 in 1 Card Reader



10/17 add for
JMB380

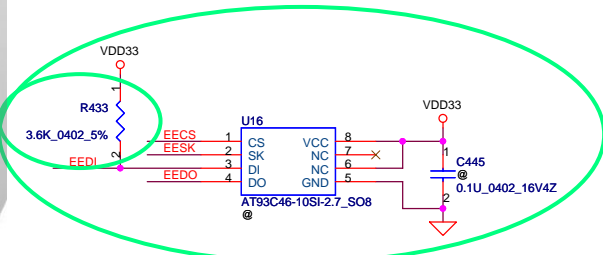
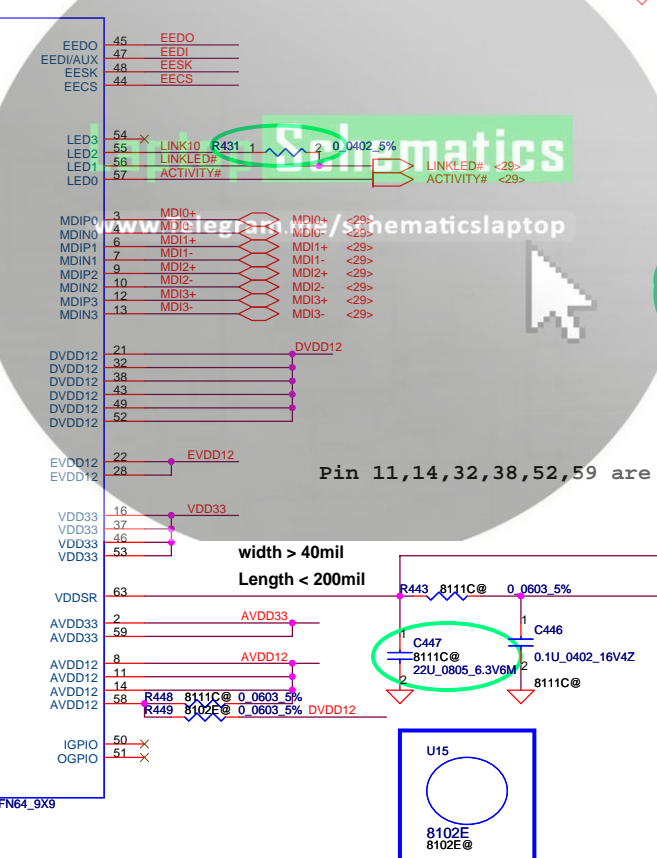
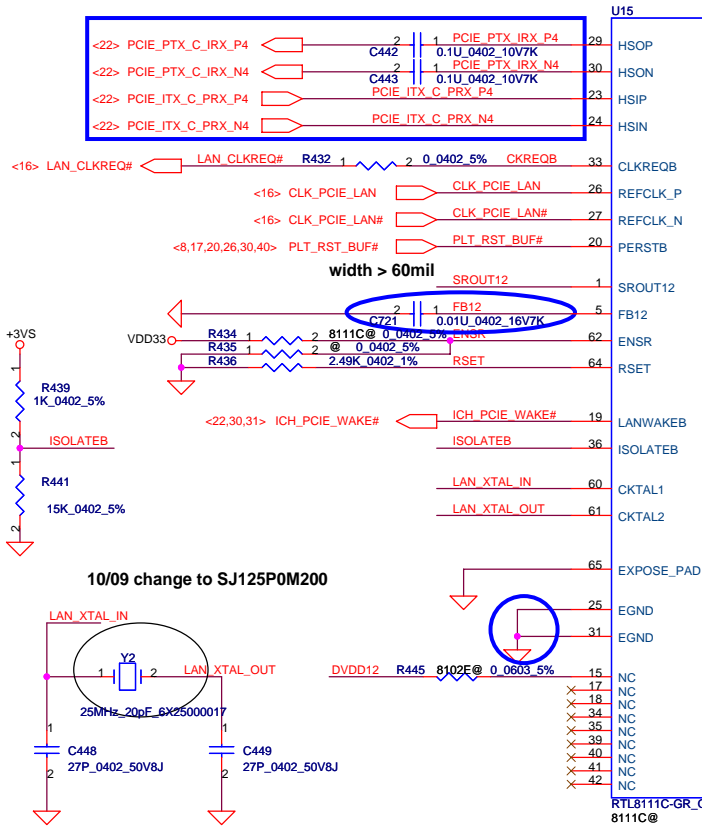
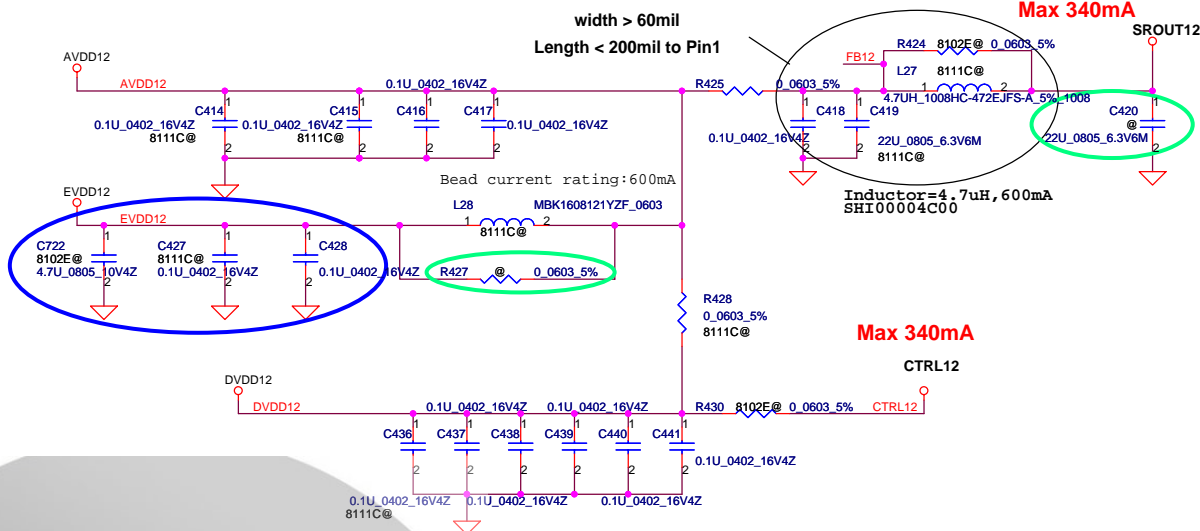
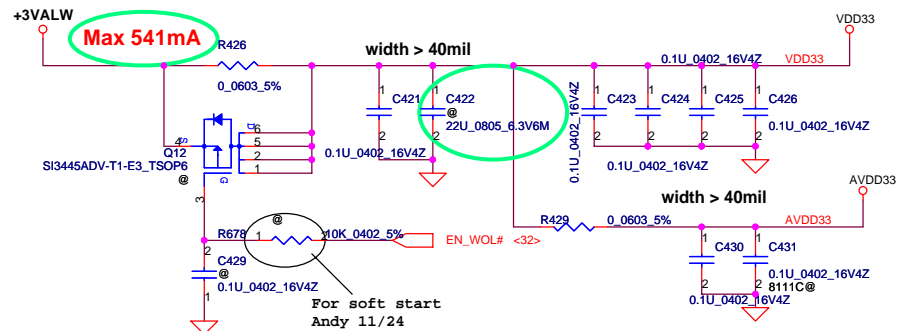


The circuit need reserve for JMB385?



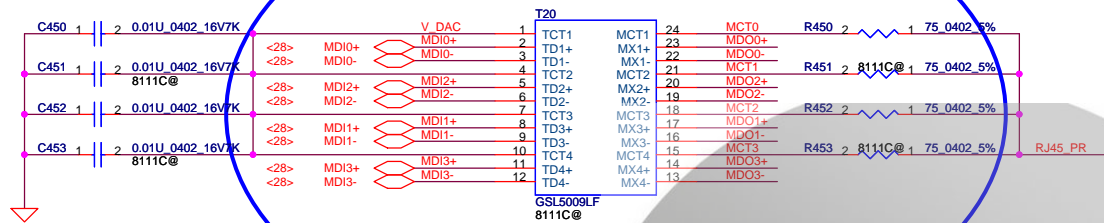
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	3 in 1 Card Reader Conn
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				Date: Friday, April 11, 2008	Rev 0.4

Printed at: print@compal.com

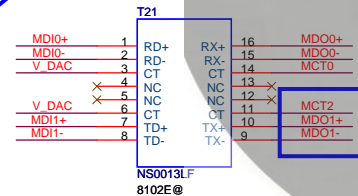


Pin 11,14,32,38,52,59 are NC pins when use 8102E

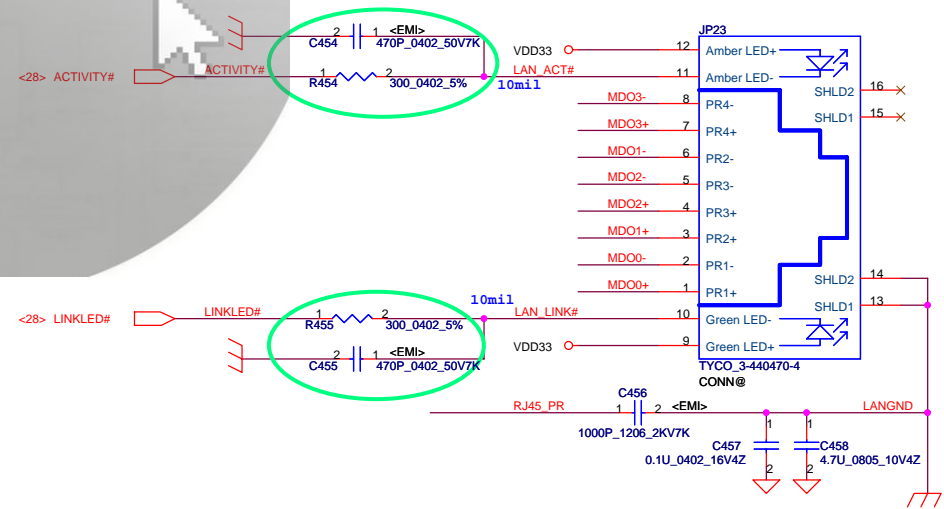
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Issued Date		2007/08/18		Deciphered Date		2008/8/18		Title						
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								Size	Document Number			Rev		
								Custor	JHXXX M/B LA-4241P Schematic			0.4		
Date:		Tuesday, June 03, 2008		Sheet		28		of 49						



3/4 Change T20 Value from 350uH_GSL5009LF to GSL5009LF
Change T20 P/N from SP050003T00 to SP050003T10



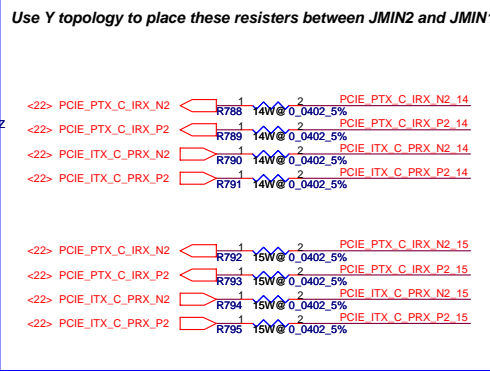
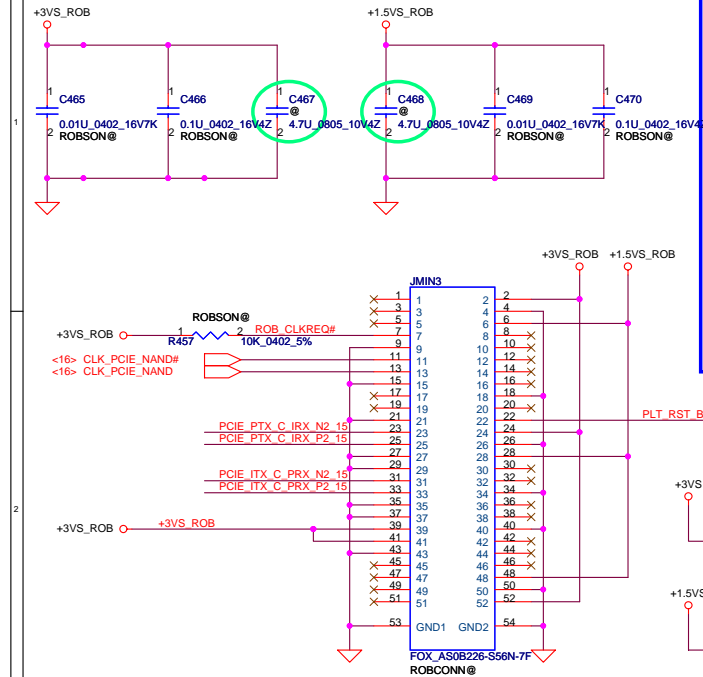
Change T21 Value from 350uH_NS0013LF to NS0013LF



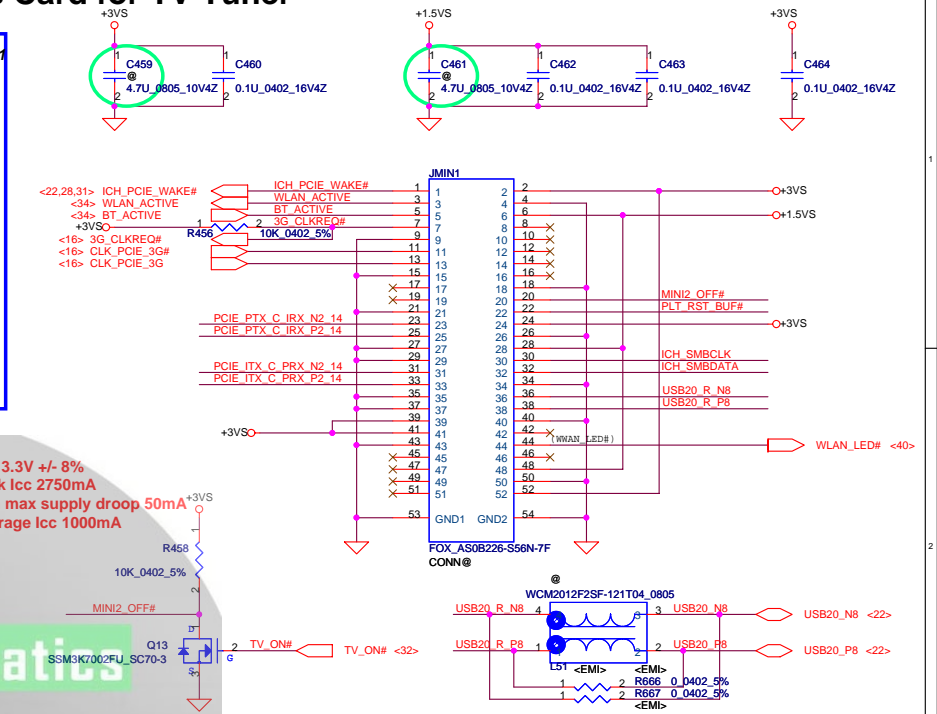
Lan Conn.

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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	LAN CONNECTOR
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Custom	JHXXX M/B LA-4241P	Schematic	0.4	Date:	Wednesday, May 28, 2008
Sheet		29		of 49	

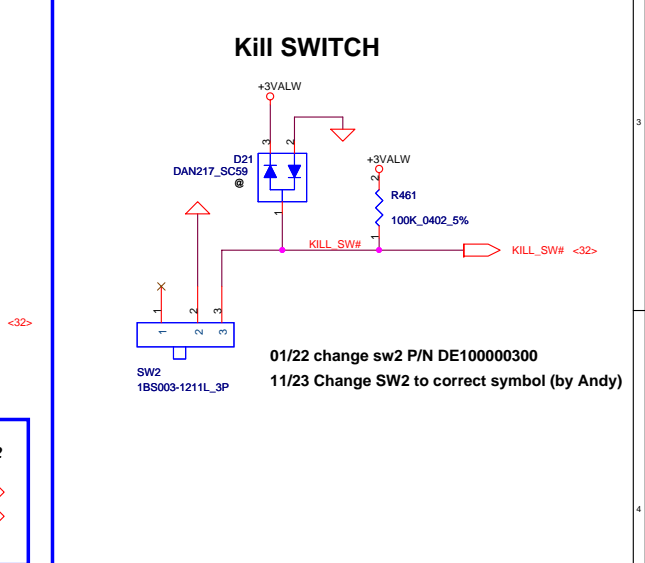
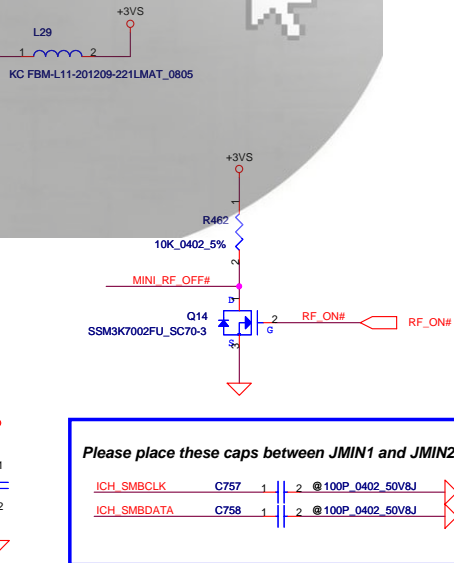
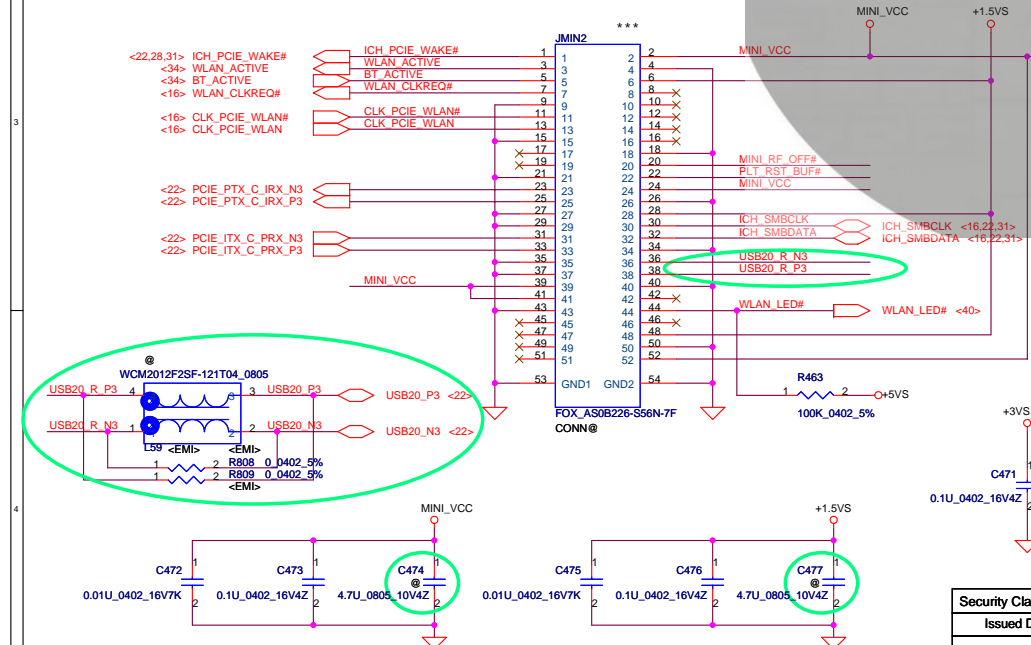
NAND mini Card(Robson support)



Mini-Express Card for TV Tuner

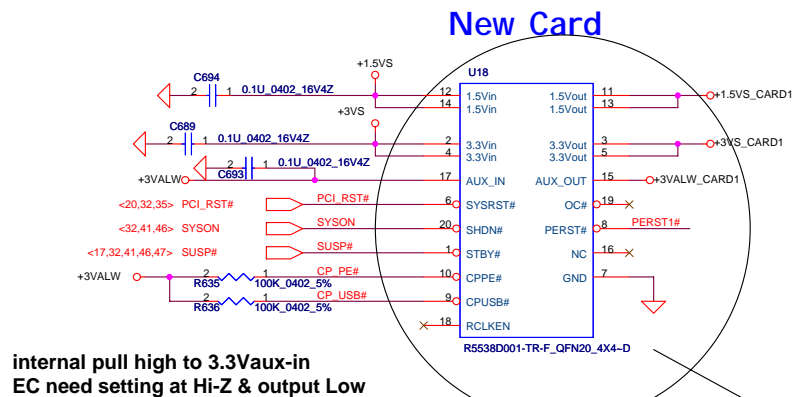


Mini-Express Card for WLAN

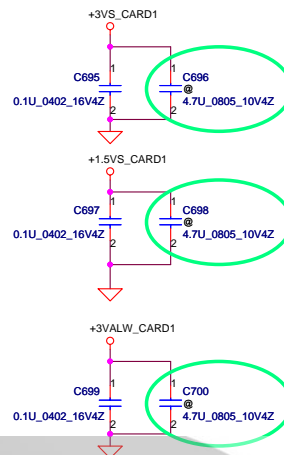


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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Mini-Card/Kill SWITCH	
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				Date	Wednesday, May 28, 2008
				Sheet	30 of 49

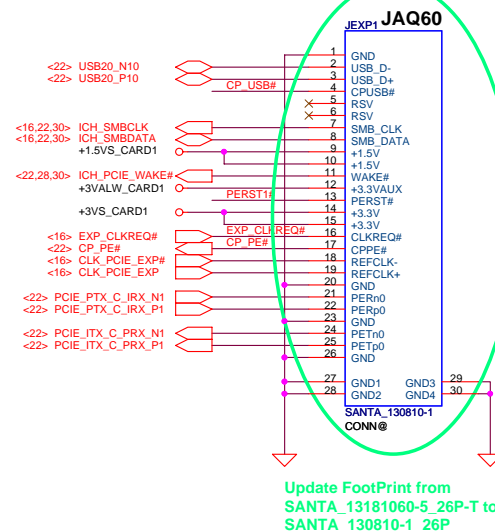
New Card Power Switch



Change to GMT PartNumber



New Card Socket (Left/TOP)



Update FootPrint from
SANTA_130810-1_26P to
SANTA_130810-1_26P-S

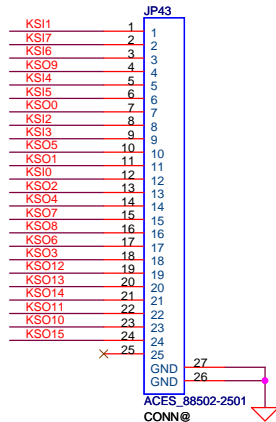
Laptop Schematics

www.Telegram.me/schematics_laptop

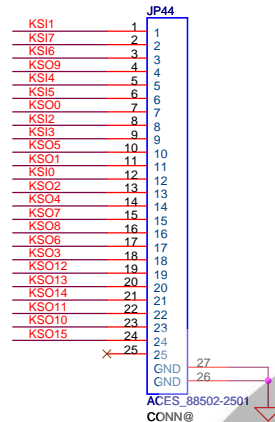
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	NEW CARD
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				JHXXX M/B LA-4241 Schematic	
				Date:	Wednesday, May 28, 2008
				Sheet	31 of 49

INT_KBD Conn.

For JHL90

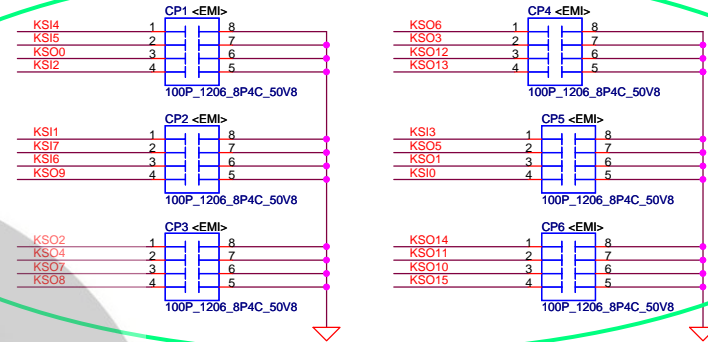


For JHT00

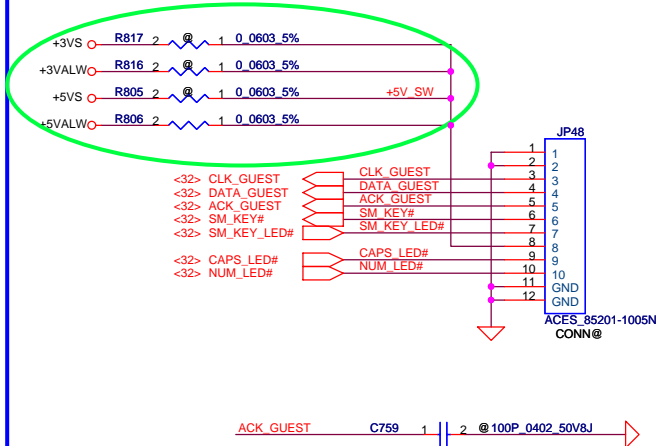


KSII[0..7] KSII[0..7] <32>
KSO[0..15] KSO[0..15] <32>

Delete C525~C548 SE071101J80 (100pF)
Add SI102101K80 (CP : 100pF)
(EMI Recommend)

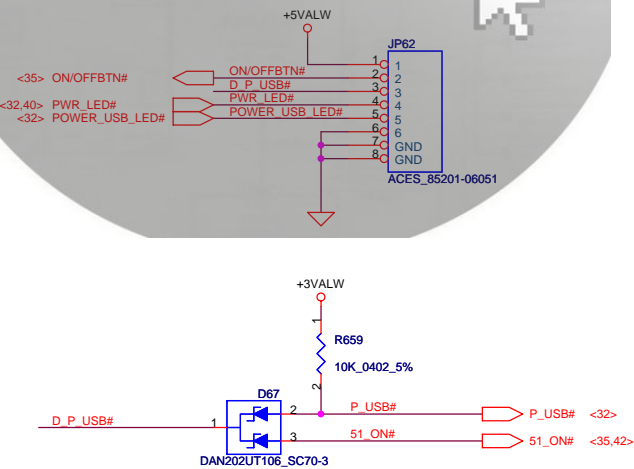


Function Board Conn.

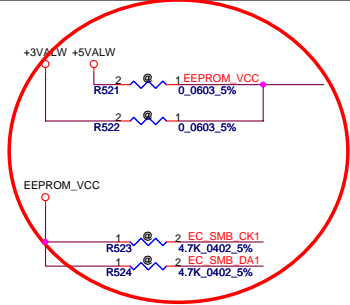


Power USB Board Conn.

www.Telegram.me/schematics1aptop

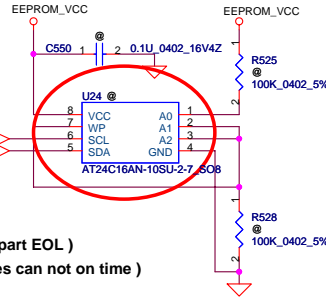


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				3	JHXXX M/B LA-4241P Schematic
				Date:	Wednesday, May 28, 2008
				Sheet	33 of 49



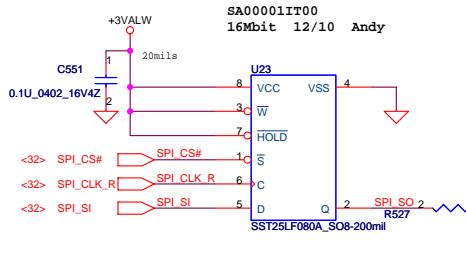
12/28 Add

0206 => change PN to SA00001N800
 12/19 change pn to SA00001MP00 (original part EOL)
 12/25 change back to SA024160140 (Samples can not on time)



16M SPI ROM

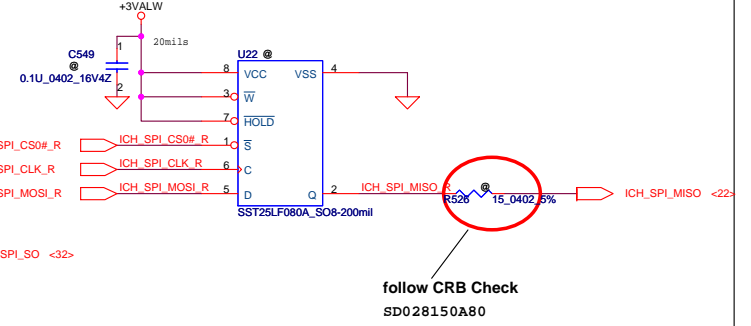
For EC+BIOS+VBIOS



12/15 change from 15 to 0 ohm'

8M SPI ROM

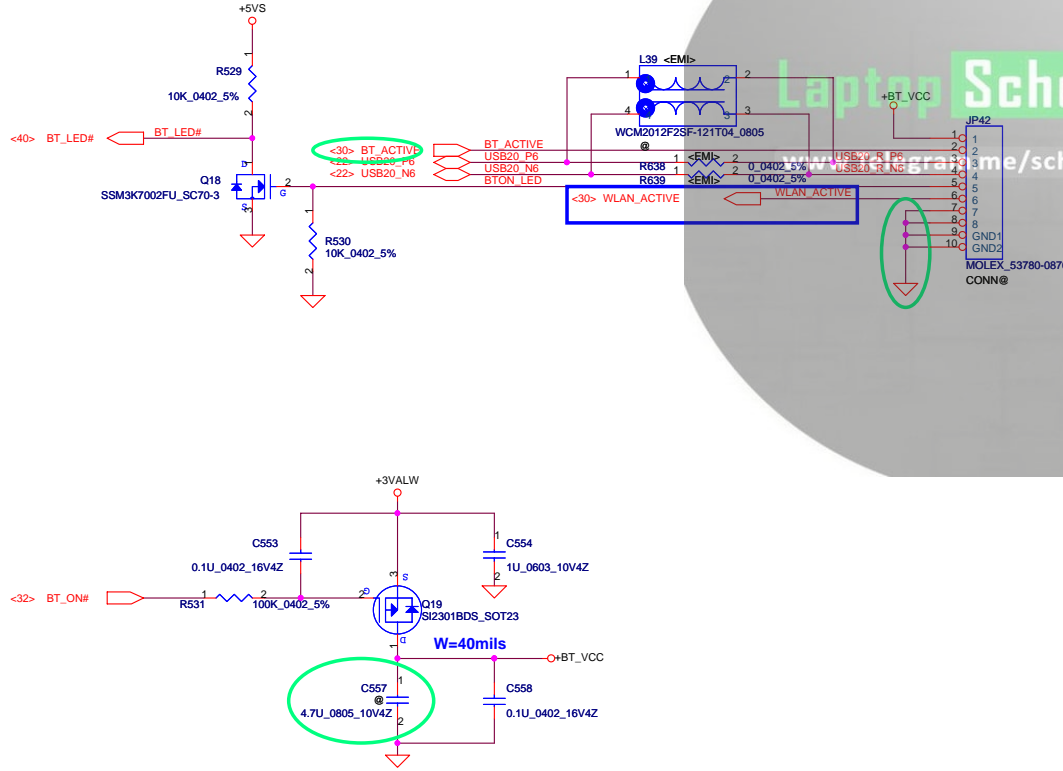
For iTPM+HDCP



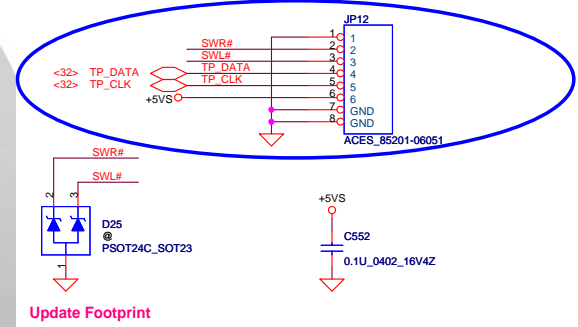
follow CRB Check
 SD028150A80

Bluetooth Conn.

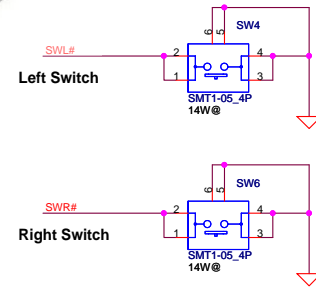
Need to check BT pin definition again!
 9/20 modified this block



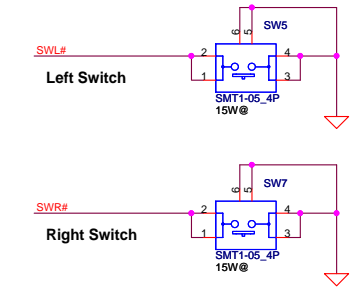
To TP/B Conn.



14W Use

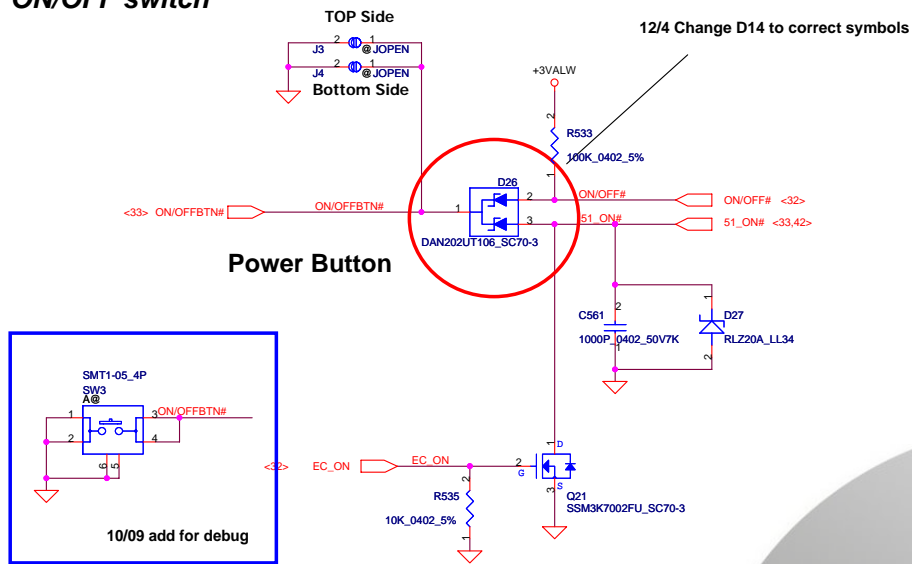


15W Use

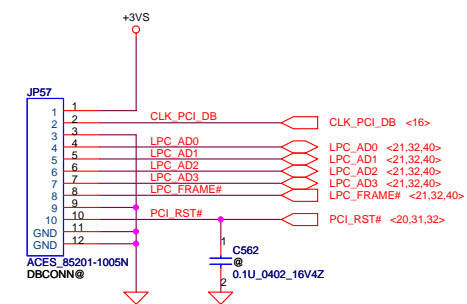


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						Size B	Document Number			JHXXX M/B LA-4241P Schematic		Rev 0.4
						Date	Wednesday, May 28, 2008		Sheet	34	of	49

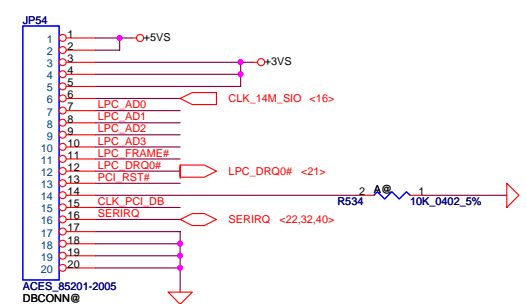
ON/OFF switch



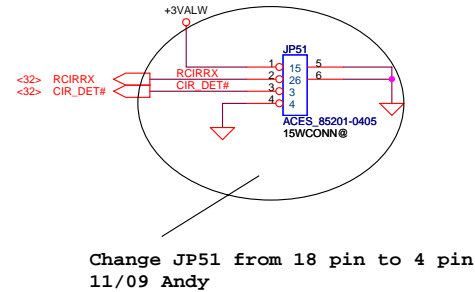
FOR LPC DEBUG PORT



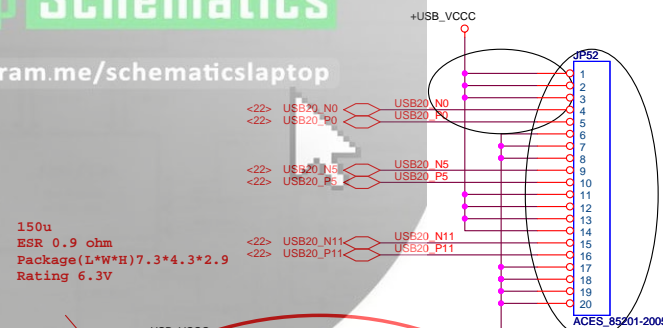
FOR LPC SIO DEBUG PORT



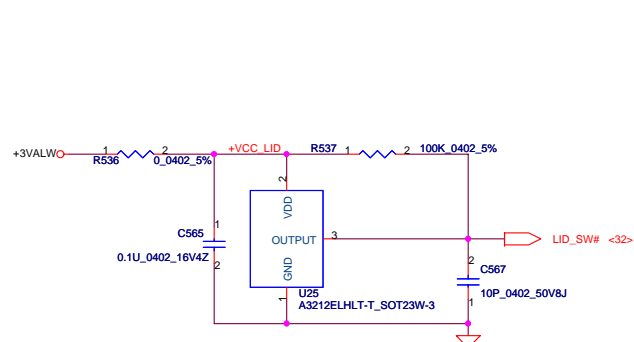
CIR



USB IO Conn.

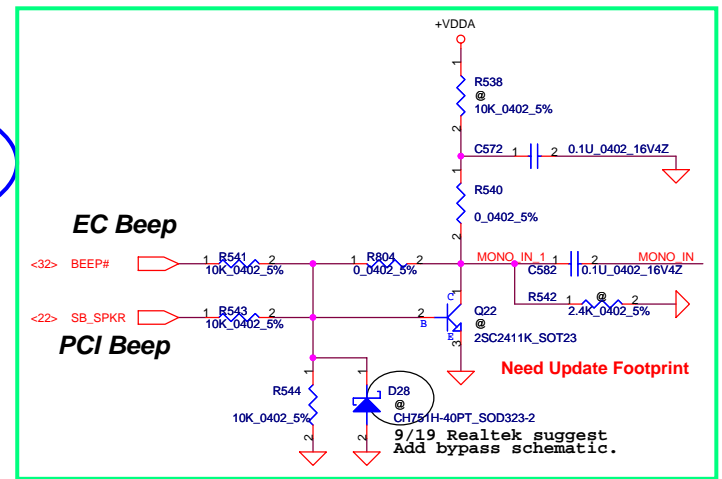
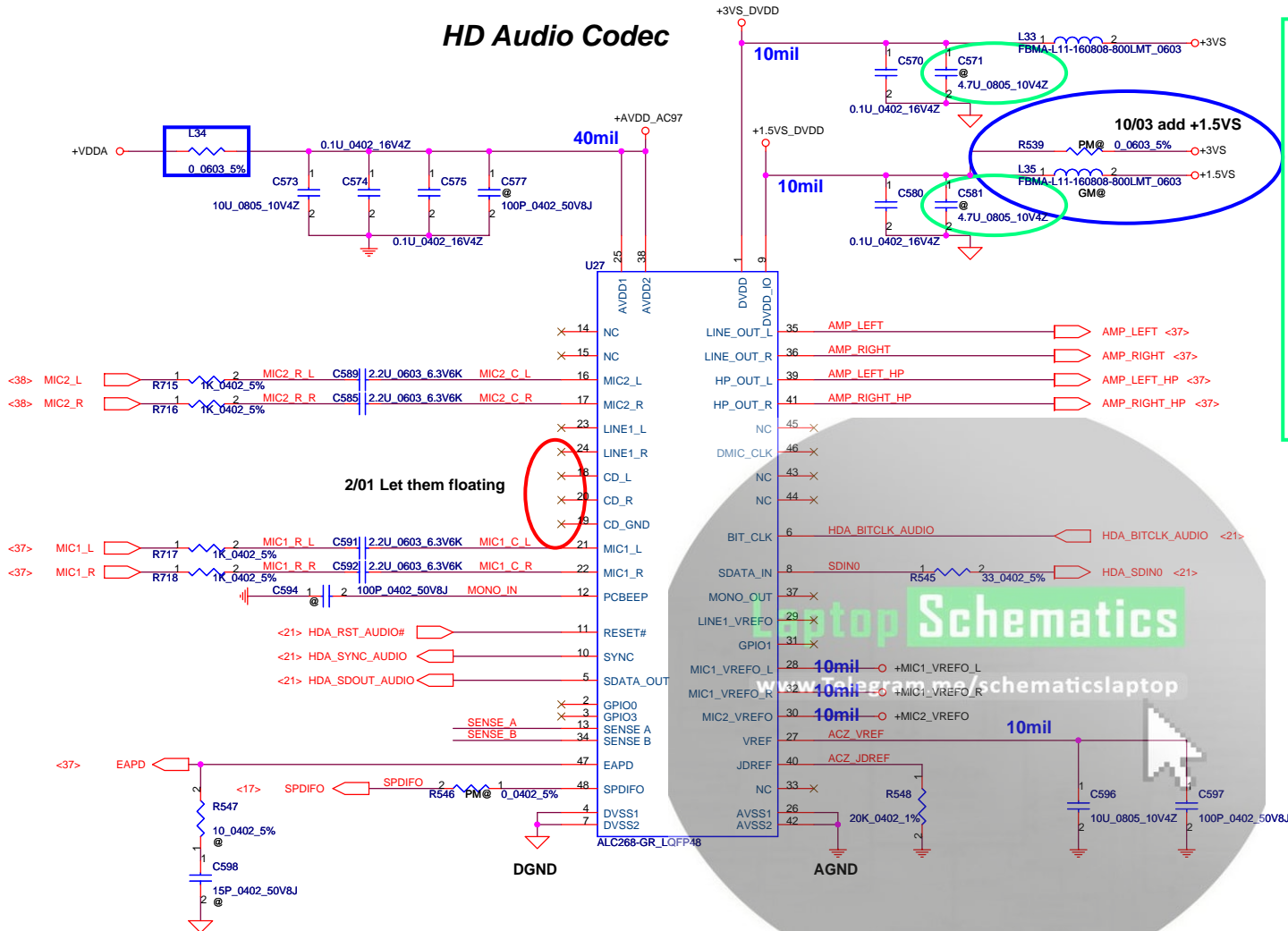


Lid Switch



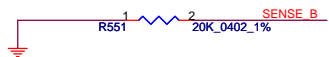
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title		Power OK/Lid/Front,IO,DB Conn	
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				B	JHXXX M/B LA-4241P Schematic	0.4	
				Date:	Wednesday, May 28, 2008	Sheet	35 of 49

HD Audio Codec

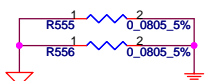


Sense Pin	Impedance	Codec Signals	Funnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE OUT
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE OUT

SENSE FOR Ext. Mic.

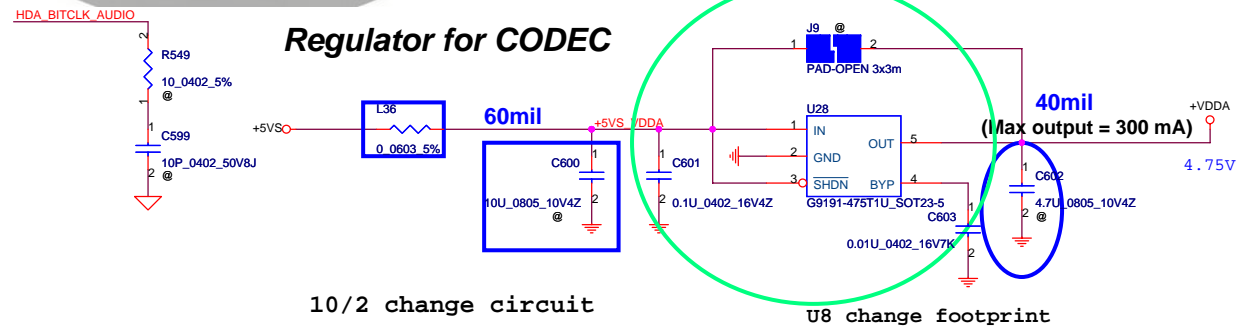
**SENSE FOR Solo Int. Mic.**

SENSE FOR HP



Moat Bridge

Regulator for CODEC



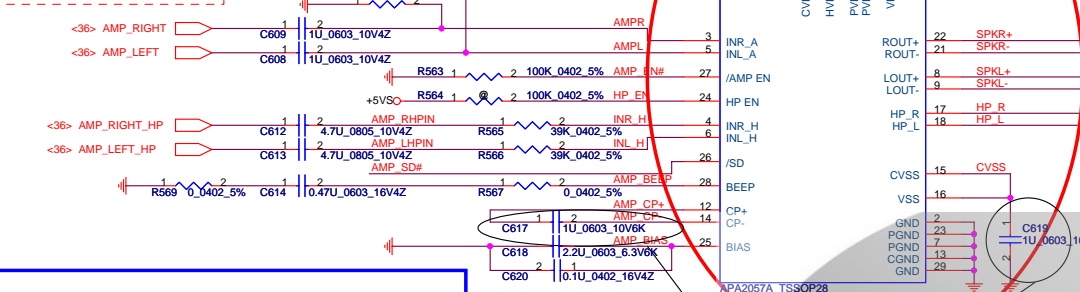
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Issued Date	2007/08/18	Deciphered Date	2008/8/18	Title	<Title> HD Audio Codec ALC268	
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APA2057 SPK/HP Amplifier

10/2 U6 APA2057A P/N:SA00001QD00

$$f_o = 1 / (2 * 3.14 * R * C) = 106\text{Hz}$$

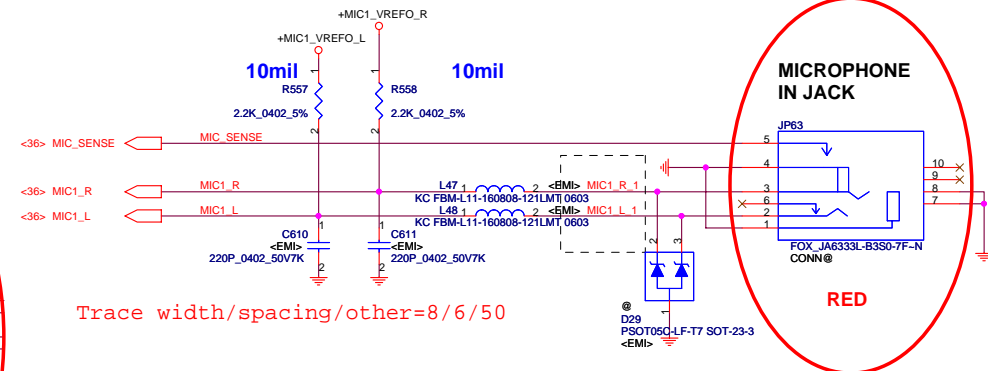
$$R = 1.5\text{K} / C = 1\mu\text{F}$$



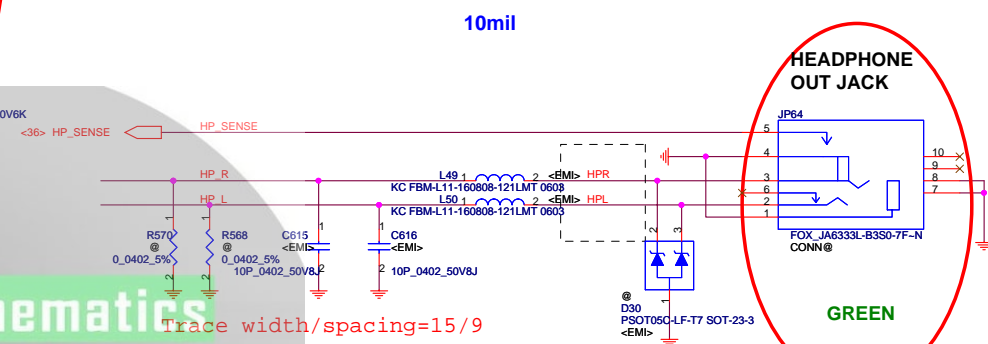
9/5 If implement AMP BEEP, Swap C641 and R524.
R524 change from 0 Ohm to 47K

IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

11/28 Modified to X5R
11/28 Change to SE080105K80

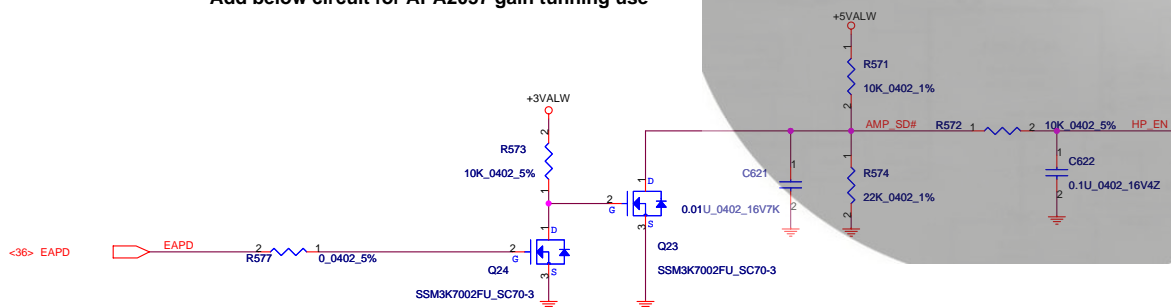


Trace width/spacing/other=8/6/50



Trace width/spacing=15/9

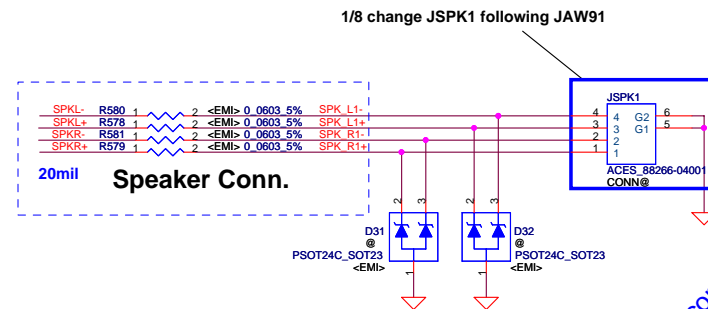
Add below circuit for APA2057 gain tuning use



Gain= 10dB

Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

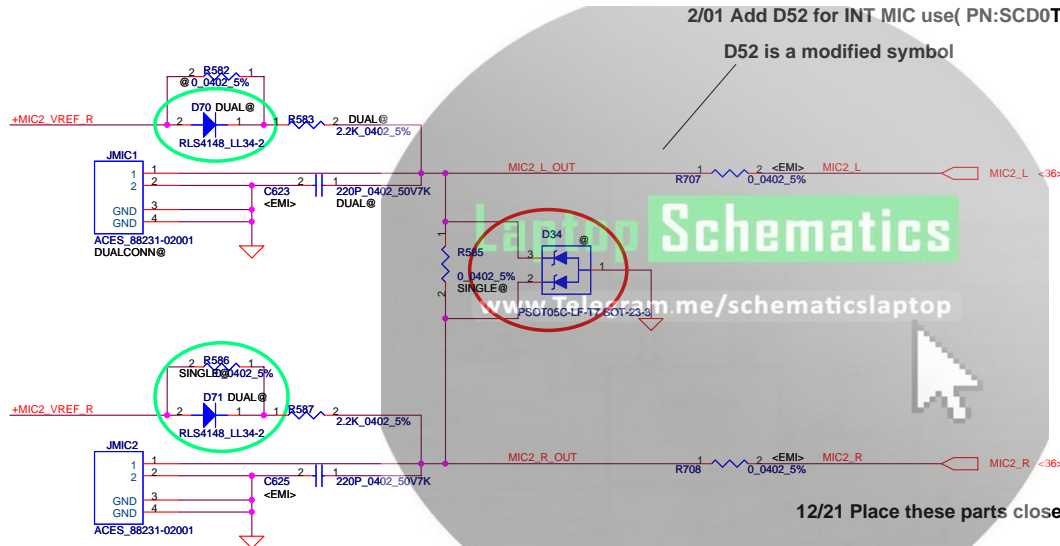
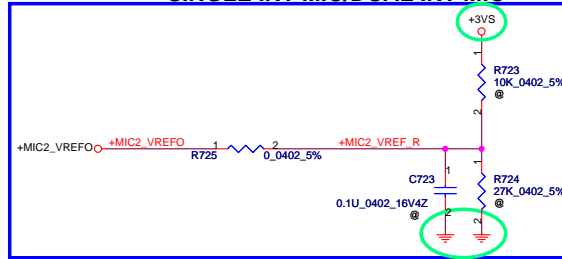
+5VALW assume equal 5.1V
10 dB ----> 5.1 x 220 / 320 = 3.5



1/8 change JSPK1 following JAW91

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SINGLE INT MIC/DUAL INT MIC



2/01 Add D52 for INT MIC use(PN:SCD0T05CA20)

D52 is a modified symbol

12/21 Place these parts close to CODEC (U7)

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Date:	Wednesday, May 28, 2008	Sheet	38	of	49

11/27 Add screw for layout request

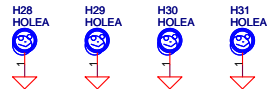
H_3P0



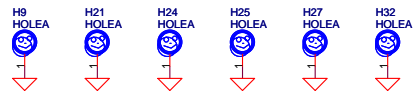
H_3P7



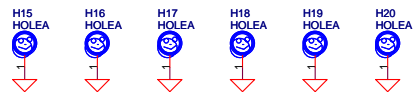
H_4P2



2/22 change these from H_3P7 to H_3P8



2/22 change these from H_3P2 to H_3P3



H_5P0X3P2N

H_5P0X3P2N



H_5P2X3P2N

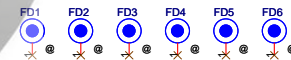
H_3P1N

H_5P0X3P2N

11/27 Add screw for layout request

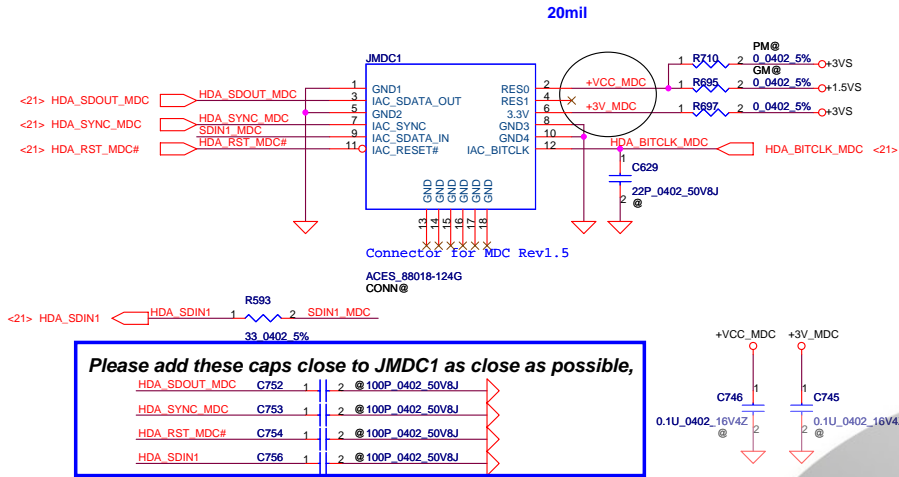
Laptop Schematics

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				JHXXX M/B LA-4241P Schematic	
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				Rev	0.4

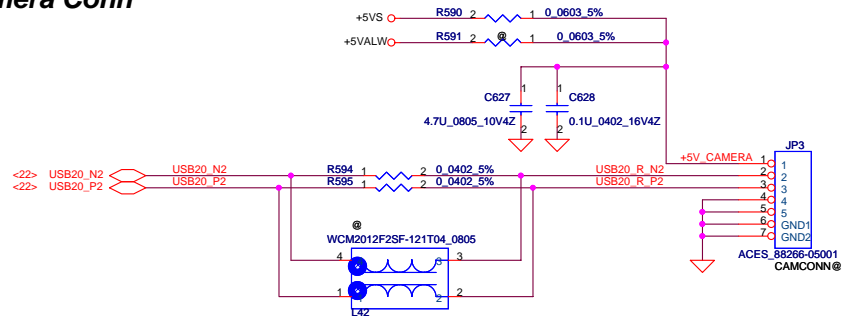
MDC Conn.



TPM X76 Information

X76 P/N	Vendor	Location	Bom Structure
X7611630L07	Infineon	C717,C718,R698,R702,R703,U32,X3	IN_TPM@
X7611630L08	Winbond	C724,U32	WB_TPM@

Camera Conn



Finger Print board

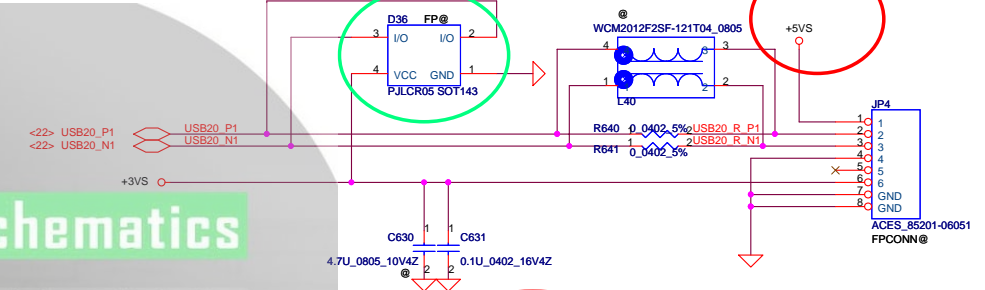
05/26 Change D36 from SC300000X00 to SC300000K00

1/05 Modified D3 to SCA00000A00 For EMI

2/1 change JP4 pin 6 to +5VS for LTT FP use

0208 Remove D3, Add D55 (SC300000G00)

EMI Request

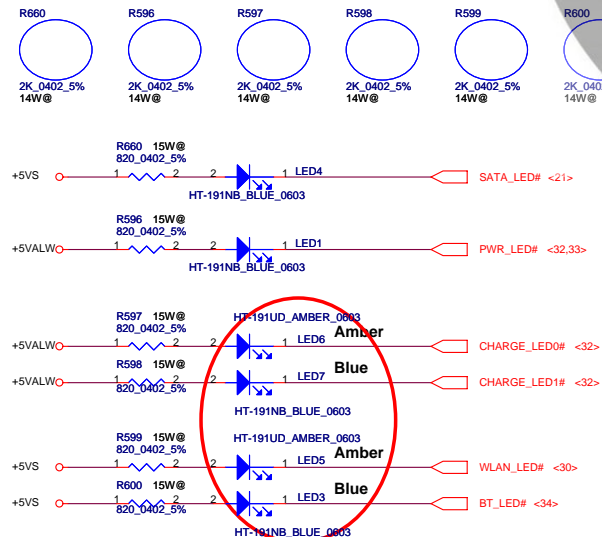


TPM 1.2

LED

05/28 Change R660,R596,R597,R598,R599,R600 to 820ohm for 15W@

05/28 Add R660,R596,R597,R598,R599,R600 to 2kohm for 14W@



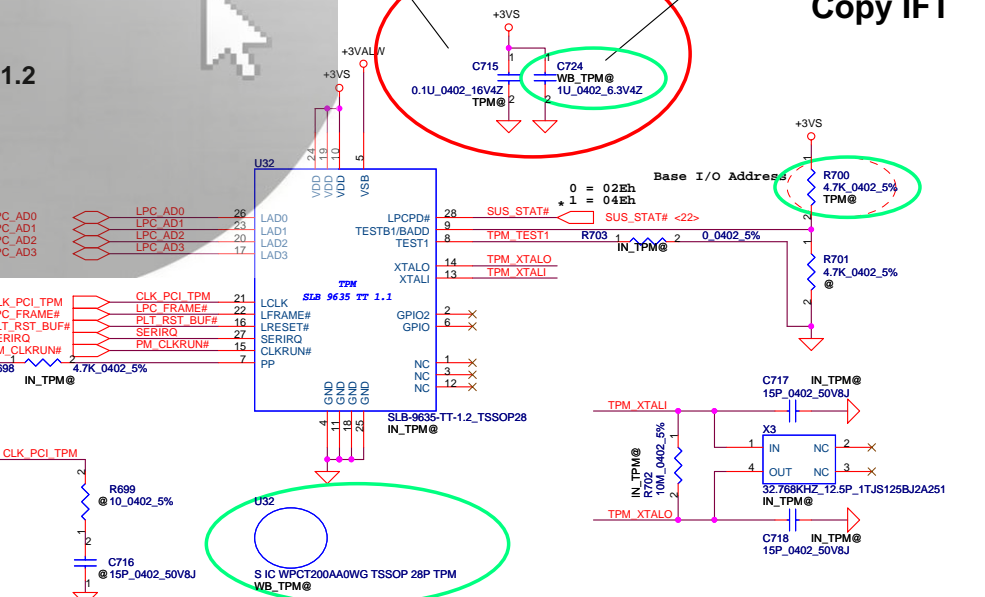
12/7 Modified LED footprint to LED_HT-297UD-CB_4P

12/15 Modified to correct LED symbol!!

Let C715 close pin 24

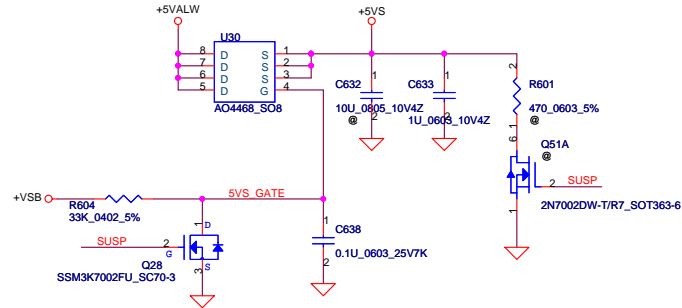
Let C724 close pin 10

Copy IFT

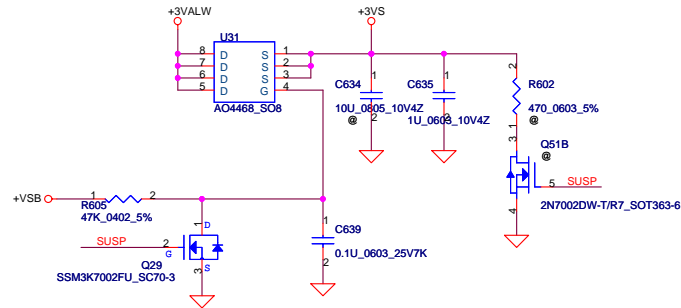


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Title				MDC/LED/Camera/FP				Rev			
Size				Document Number				JHXXX M/B LA-4241P Schematic			
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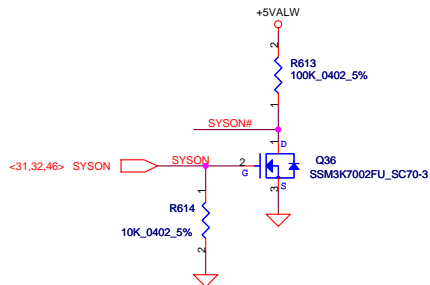
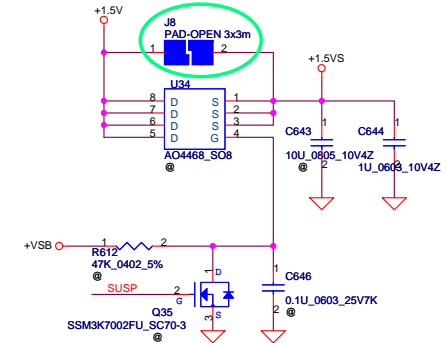
+5VALW TO +5VS



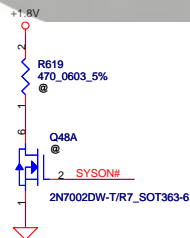
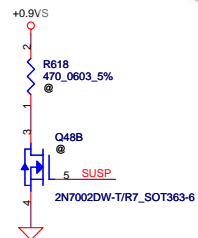
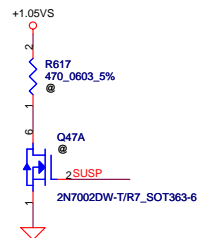
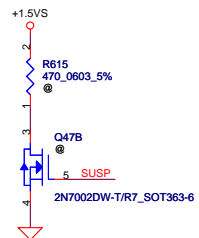
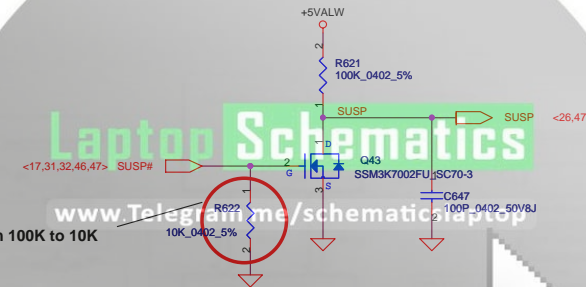
+3VALW TO +3VS



+1.5V TO +1.5VS

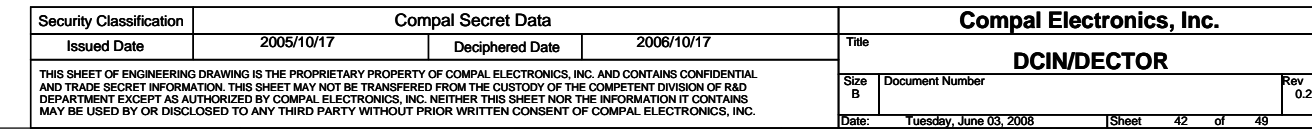


3/14 Change R16 from 100K to 10K

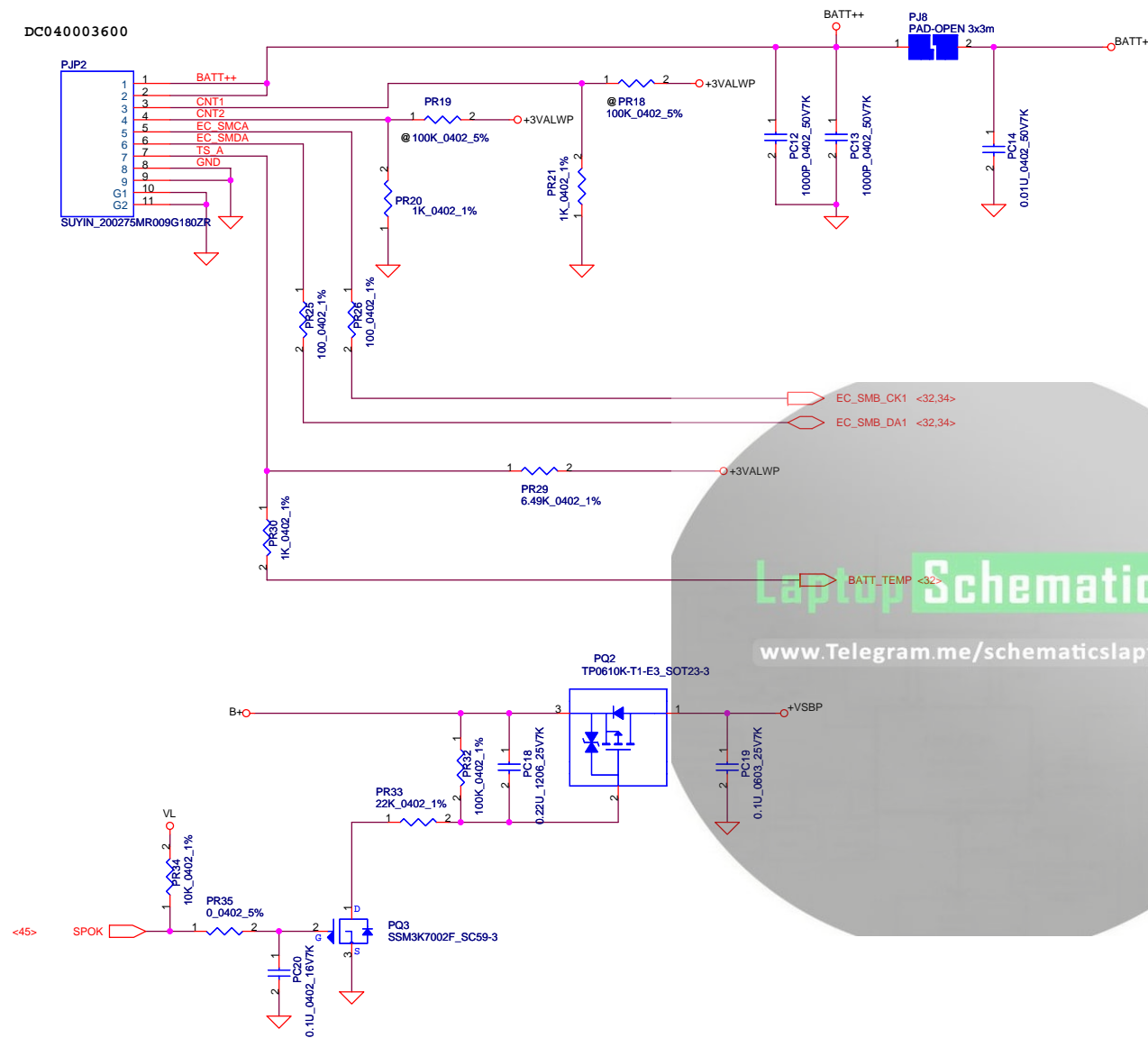


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								2008/8/18			
								Title			
								DC Interface			
								Document Number			
								JHXXX M/B LA-4241P Schematic			
								Date: Wednesday, May 28, 2008			
								Sheet 41 of 49			

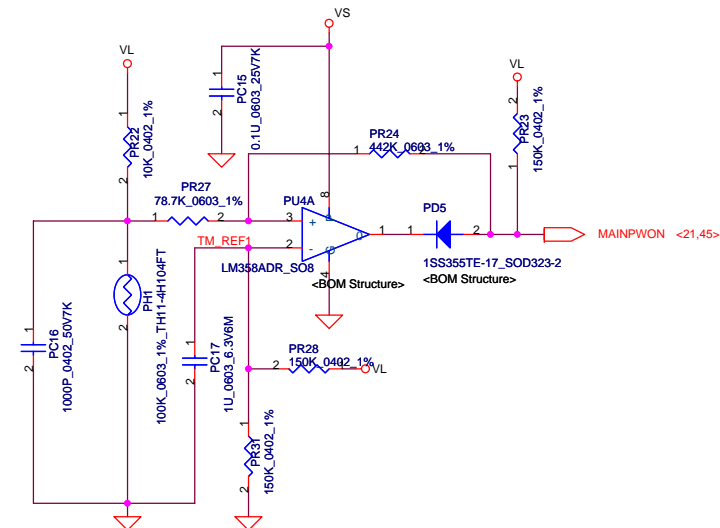
© SINGA 2DW-0268-B16



DC040003600



PH1 under CPU bottom side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C

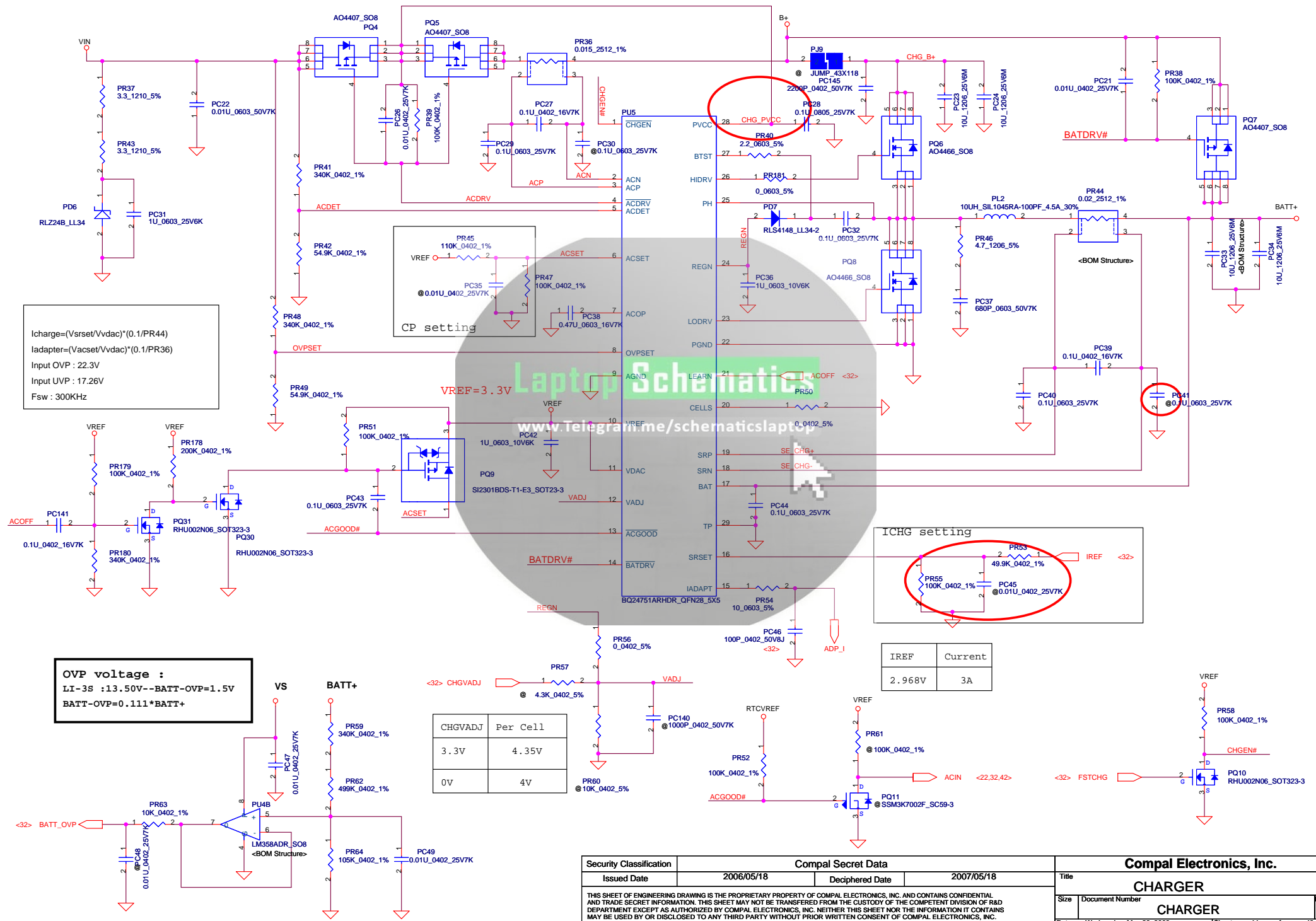


Laptop Schematics

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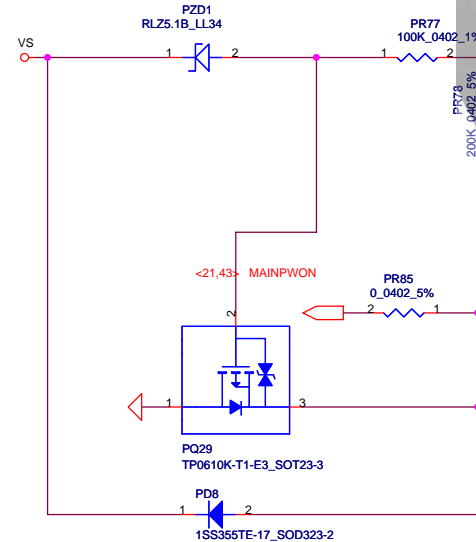
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Size B	Document Number	Rev 0.1			Date: Tuesday, June 03, 2008
Sheet 43		of 49		hexamail.com	

65W, Iadapter=0~3.42A, Current sense=0.015ohm, PR45=110K, CP=3.175A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR45=54.9K, CP=4.303A



$R_{ds(on)} = 18\text{m ohm(max)} ; R_{ds(on)} = 15\text{m ohm(typical)}$

3.3VALWP
 $I_{max}=5.59\text{A}$
 $I_{peak}=7.85\text{A}$
 $I_{ocp}=10.133\text{A}$

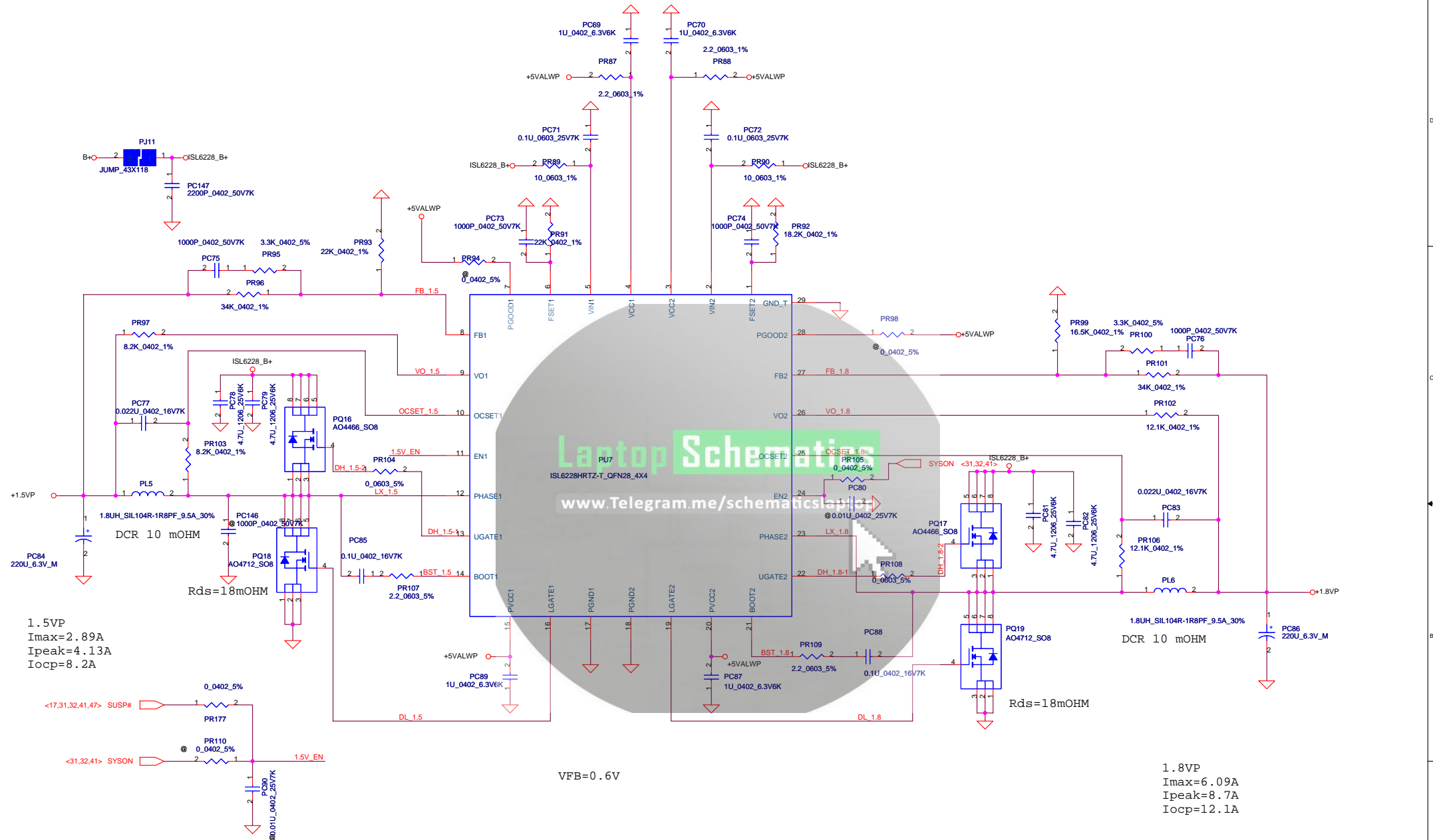


<21,43> MAINPWON

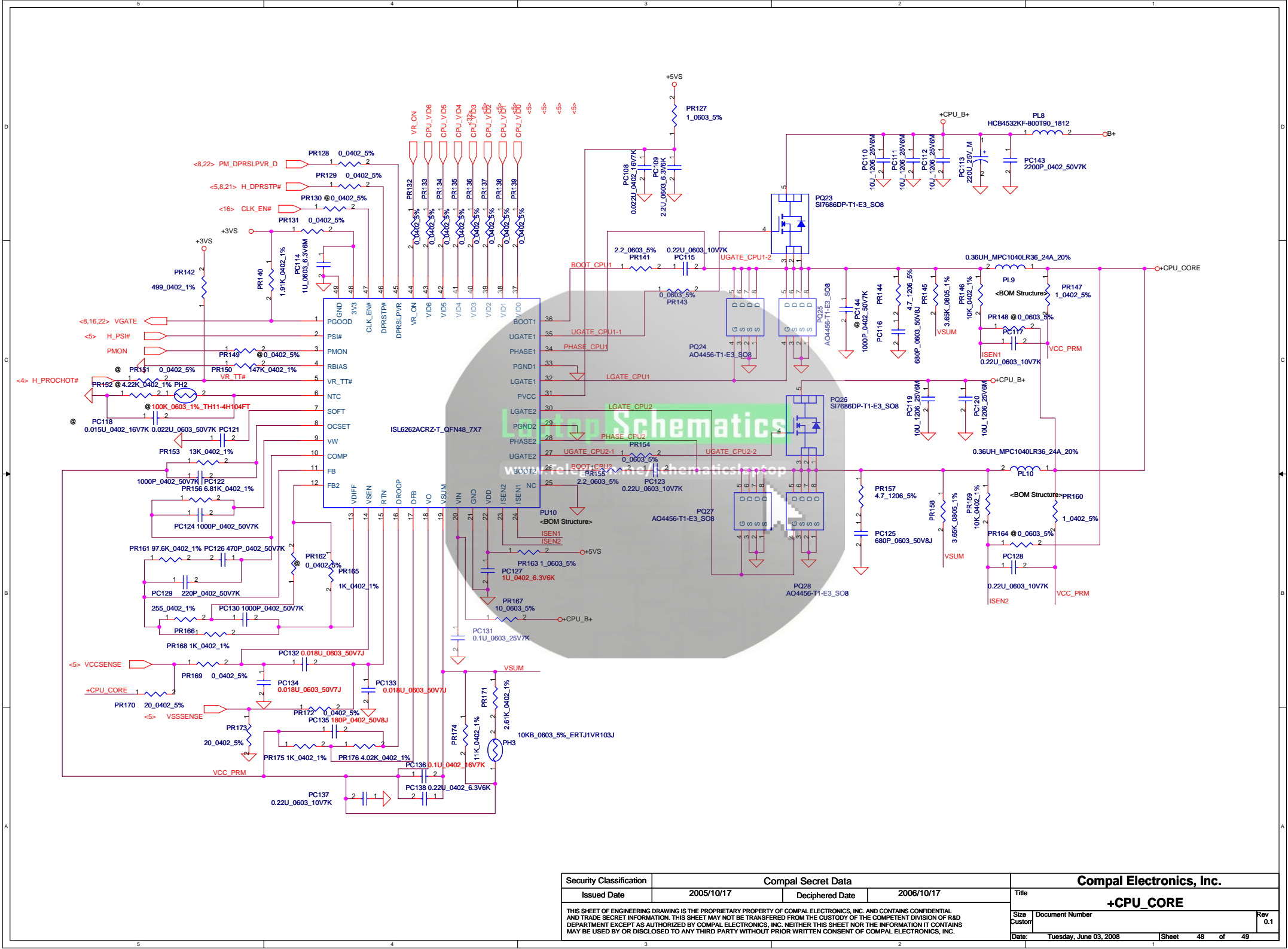
$R_{ds(on)} = 18\text{m ohm(max)} ; R_{ds(on)} = 15\text{m ohm(typical)}$

5VALWP
 $I_{max}=4.9\text{A}$
 $I_{peak}=7\text{A}$
 $I_{ocp}=10.146\text{A}$

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Size	Document Number	Custom		Rev	0.1
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				Size	Document Number	Rev
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				Date: Wednesday, May 28, 2008		
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page	Reason for change	Modify list
	Add original ACIN detector fun,and del TI fun.	ADD PR6, Del PQ11, PR61
	Change PC28 to 0.1U for common design	PC28
	Change PR16,PR32 & PR77 to 1% for common part	PR16 & PR32 & PR77
	Change PC55 to 0.1U_0603 for common design	PC55
	Add PC139 for 3/5V 2nd source	PC139
	Change PQ21 to A04712 and PL7 to 1.8UH for cost	PQ21 & PL7
	Change PC12 and PC13 to 0402 for source suggest	PC12 & PC13
	Change PR176 to 4.02K for load line	PR176
	Change 1.05V VIN from 5valwp to 5VS. reduce S3 power loss	
	Del PR83 for extra pull-high R	
	Add cpu_core boost and sunnber for EMI request	Add PR141,PR144,PC116,PR155,PR157 &PC125
	Add 1.05VSP boost and sunnber for EMI request	Add PR113,PR117 &PC98
	Fixed CV mode	Add PR56,Del PR57&PR60
	Adjust 1.05V to 1.074 for HW request	Modify PR120 to 2.37K
	Adjust 1.5V to 1.527 for HW request	Modify PR93 to 22K
DVT	Del PR73 for fix 3V in 2nd source	
	Add PQ30,PQ31, PR178,PR179,PR180,PC141	Prevent ACOP protection by charger
	Modify PQ10 to SOT322	Layout limit
	Modify 1.5V to susp#	Add PR177, Del PR170
	Modify PR36 to 0.015 for rating & change PR45 to 100K	
	Modify PL9 & PL10 form NEC to TOKO	
	Modify PR108 to 2.2 for EMI request	
PVT	Fix 5valwp, so del PR71, change PR72 to 0	
	Change PC8 to Y5V type for costdown	
	Change PU6 & PC101 to PU500 &PC500 for BOM	
	Add PC142,PC143,PC144,PC145,PC146,PC147,PC149,PC150 for EMI request	
	Add PR40,PR181,PR107,PR109,PR46,PC37 & Del PR108 for EMI request	
	Change PQ24,PQ25,PQ27,PQ28 to A04456 for EOL	
PVT-1	Move PC500 & PU500 to X76 group.	
Pre-MP	Del PC144 & PC146 for EMI request	

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